An Improved PWM Strategy for Z-Source Inverter With Maximum Boost Capability and Minimum Switching Frequency

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Abstract—Z-source inverter provides a competitive single-stage dc–ac power conversion with the capability of both buck and boost voltage regulation. In order to maximize voltage gain and to increase efficiency, this paper proposes an improved pulse-width modulation (PWM) strategy. By adjusting the shoot-through duty ratio of one-phase leg, it regulates the average value of intermediate dc-link voltage, which is the same as the instantaneous maximum of three-phase line voltage in one switching time period (T_s). And the other two-phase legs maintain the fixed switching states. Thus, the equivalent switching frequency of power devices in the inverter bridge is reduced to $1/3 f_s$ (f_s is the frequency corresponding to T_s). The operating principles and closed-loop controller design are analyzed and verified by simulation and experiments. Compared with the existing PWM strategies, the improved PWM (IPWM) strategy demonstrates higher efficiency under full operation range of low voltage gain (1.27-2) application. However, with the IPWM strategy, the inductor current and capacitor voltage contain six-time-line-frequency ripples, which consequently require large size of the passive components when the output frequency is very low. Thus, it is also suitable for 400–800-Hz medium frequency aircraft and vessel power supply system due to a relatively high output line frequency. Furthermore, the idea of IPWM strategy can be extended to other kinds of three-phase impedance network-based inverters.

Index Terms—Closed-loop control, dc/ac conversion, minimum switching frequency, pulse-width modulation (PWM) strategy, voltage gain, Z-source inverter.

I. INTRODUCTION

CONVENTIONAL two-level three-phase voltage source inverter (VSI) can only perform buck voltage regulation.

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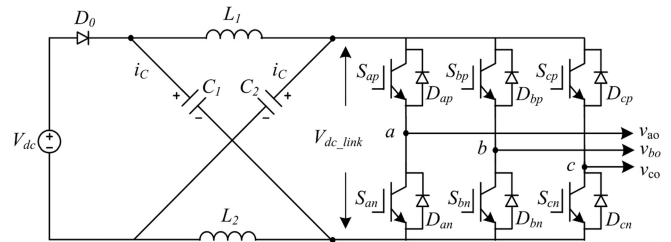Digital Object Identifier 10.1109/TPEL.2017.2661321

Fig. 1.   Z-source inverter.

For applications requiring both buck and boost power conversion, an additional boost dc–dc converter is required in the front. In view of two-stage power conversion increasing system cost and lowering efficiency, Peng [3] proposed Z-source inverter, shown in Fig. 1, introducing a unique impedance network between the source and the inverter bridge. It achieves voltage boost capability by advantageously adopting shoot through (ST) of inverter-bridge legs, which provides a potential low-cost, high-efficiency, and single-stage power conversion when the boost ratio is low (1–2) [33]. Furthermore, the ST permission of inverter-bridge legs and elimination of dead-zone time are beneficial to improve the system reliability and quality of output waveforms. Since Z-source inverter overcomes the limitations of traditional VSI, various new topologies [4]–[14], pulse-width modulation (PWM) strategies [15]–[26], and model and control methods [27]–[31] were proposed to improve its performance.

The existing widely used PWM strategies for Z-source inverter include simple constant boost control (SCPWM) [3], maximum boost control (MPWM) [16], and maximum constant boost control (MCPWM) [17], according to the intermediate dc-link voltage utilization. SCPWM uses carrier wave based sinusoidal pulse width modulation (SPWM), and it has the drawback of insufficient dc-link voltage utilization. In order to increase voltage gain as well as to reduce voltage stress of switching devices, Peng *et al.* [16] proposed MPWM, which utilizes all the zero states for ST interval. However, the periodic ST interval causes the six-time-line-frequency (6ω) ripples in the dc-side impedance network. In order to alleviate the undesired influence of low-frequency ripples, Shen *et al.* [17] proposed MCPWM with fixed ST interval. According to the distribution
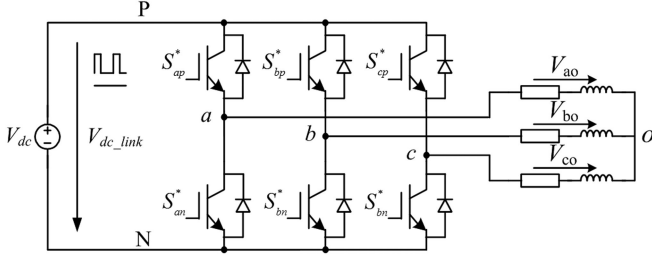
Fig. 2. Three-phase VSI.

Fig. 3. Equivalent modulation waveforms of carrier wave-based SPWM and SVM.

of ST current in three-phase legs, there are two major categories: single-phase leg ST (1P ST) and three-phase leg ST (3P ST) [19], [20]. 1P ST method inserts ST interval by overlapping the upper and lower switches in each phase leg at every switching commutation. Thus, the ST interval is averagely divided into six parts in one switching time period (T_s), which is beneficial to reduce the volume of inductors considerably. 3P ST method inserts ST interval in three-phase legs simultaneously, which is beneficial to reduce the current stress and conduction loss of power devices. However, it introduces an additional switching commutation.

This paper starts by reviewing typical PWM strategies of Z-source inverter through modification of the conventional VSI PWM strategies [e.g., SPWM and space vector modulation (SVM)] in Section II, and then proposes an improved PWM (IPWM) strategy with maximum voltage gain and minimum switching frequency in Section III. By adjusting the ST duty ratio of one phase leg, it regulates the average value of intermediate dc-link voltage, which is the same as the instantaneous maximum of three-phase line voltage in one switching time period (T_s). As a result, the equivalent switching frequency of power devices in the inverter bridge is reduced to $1/3 f_s$ $(f_s = 1/T_s)$, which makes a great contribution to the reduction of switching losses. After that, a comprehensive comparison between the IPWM strategy and existing PWM strategies is carried out in terms of power device and passive component requirements in Section IV. The detailed closed-loop controller design is investigated in Section V. Simulation and experiment verification are presented in Section VI. The conclusion of this study is outlined in Section VII.

II. TYPICAL PWM STRATEGIES OF Z-SOURCE INVERTER

The aforementioned PWM strategies including SCPWM, MPWM, and MCPWM can use either 1P ST or 3P ST. They are referred as SCPWM + 1P ST, SCPWM + 3P ST, MCPWM + 1P ST, MCPWM + 3P ST, MPWM + 1P ST, and MPWM + 3P ST in this study. Usually, all these six typical PWM strategies can be derived by modifying the modulation waveforms of conventional three-phase VSI.

Figs. 2 and 3 show the main circuit of conventional three-phase VSI and three typical PWM strategies including SPWM, SPWM with 3rd harmonic injection (SPWM + 3rd) or SVM. Three-phase symmetrical output voltage and output power can be expressed as follows:
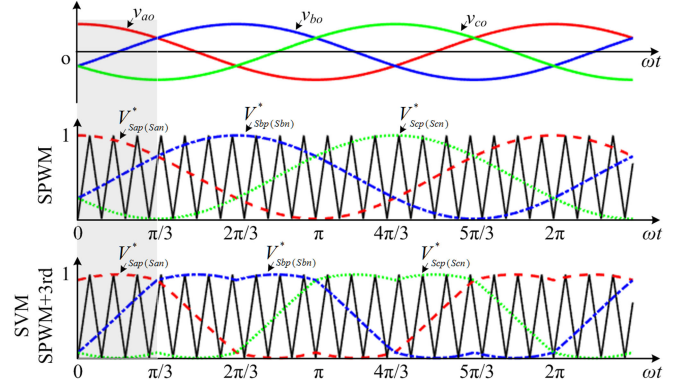
$$
\begin{cases}
v_{\text{ao}}(\omega t) = \hat{v}_{\text{ac}} \cdot \cos(\omega t) \\
v_{\text{bo}}(\omega t) = \hat{v}_{\text{ac}} \cdot \cos\left(\omega t - \frac{2}{3}\pi\right) \\
v_{\text{co}}(\omega t) = \hat{v}_{\text{ac}} \cdot \cos\left(\omega t + \frac{2}{3}\pi\right)
\end{cases}
\tag{1}
$$

$$
P_o = \frac{3}{2} \cdot \hat{v}_{\text{ac}} \cdot \hat{i}_{\text{ac}} \cos(\varphi)
\tag{2}
$$

where $\hat{v}_{\text{ac}}$ and $\hat{i}_{\text{ac}}$ are the peak value of phase voltage and current, $\cos(\varphi)$ is the load power factor, $\omega = 2\pi f_{\text{line}}$, and f_{line} is the fundamental frequency of output phase voltage.

The voltage gain, as well as modulation index, is defined as $\hat{v}_{\text{ac}}$ over half of dc-link voltage

$$
M_i = \frac{\hat{v}_{\text{ac}}}{v_{\text{dc}}/2}.
\tag{3}
$$

As is shown in Fig. 3, based on the assumption that the amplitude of triangular waveform is normalized, the expressions of three-phase modulation waveforms for SPWM and SVM (in the first sextant) are expressed as (4) and (5), respectively. Compared with SPWM, SVM can increase the Modulation index to $2/\sqrt{3}$

$$
\begin{cases}
V^*_{\text{Sap(San)}}(\omega t) = \frac{1}{2} + \frac{M_i}{2} \cdot \cos(\omega t) \\
V^*_{\text{Sbp(Sbn)}}(\omega t) = \frac{1}{2} + \frac{M_i}{2} \cdot \cos\left(\omega t - \frac{2}{3}\pi\right) \quad \text{For SPWM} \\
V^*_{\text{Scp(Scn)}}(\omega t) = \frac{1}{2} + \frac{M_i}{2} \cdot \cos\left(\omega t + \frac{2}{3}\pi\right)
\end{cases}
\tag{4}
$$

where $0 \leq M_i \leq 1, 0 \leq \omega t \leq 2\pi$.

$$
\begin{cases}
V^*_{\text{Sap(San)}}(\omega t) = \frac{1}{2} + \frac{\sqrt{3}M_i}{4} \cdot \cos\left(\omega t - \frac{\pi}{6}\right) \\
V^*_{\text{Sbp(Sbn)}}(\omega t) = \frac{1}{2} - \frac{3M_i}{4} \cdot \cos\left(\omega t + \frac{\pi}{3}\right) \quad \text{For SVM} \\
V^*_{\text{Scp(Scn)}}(\omega t) = \frac{1}{2} - \frac{\sqrt{3}M_i}{4} \cdot \cos\left(\omega t - \frac{\pi}{6}\right)
\end{cases}
\tag{5}
$$

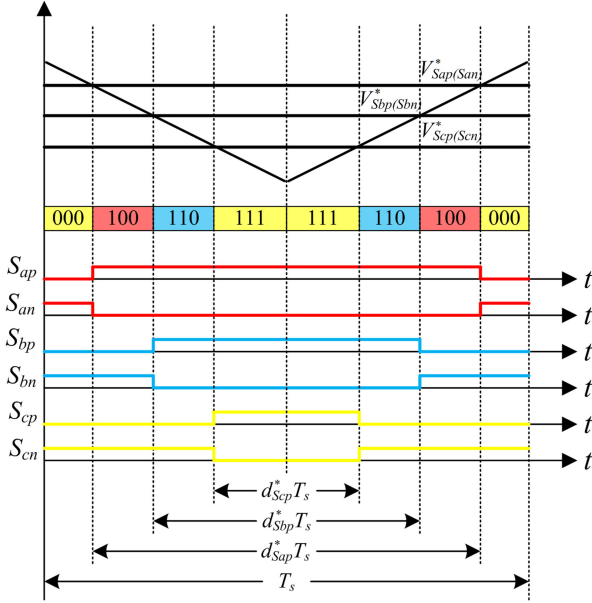where $0 \leq M_i \leq \frac{2}{\sqrt{3}}, 0 \leq \omega t \leq \frac{\pi}{3}$.

Fig. 4.   Switching states of SPWM or SVM in the first sextant ($0 \leq \omega t \leq \pi/3$).

Fig. 4 shows the switching state of SPWM or SVM in the first sextant. The comparison results of modulation waveforms and triangular wave are adopted to control the switching state of the upper and lower switches in each phase. Thus, the on-state duty ratio of upper and lower switches are $d_{\mathrm{Sip}}^*(\omega t) = V_{\mathrm{Sip}}^*(\omega t)$ and $d_{\mathrm{Sin}}^*(\omega t) = 1 - V_{\mathrm{Sip(Sin)}}^*(\omega t)$ (i represents a, b, or c).

As described in Peng [3], voltage gain of Z-source inverter is defined as the ratio of the peak phase voltage $\hat{v}_{\mathrm{ac}}$ over half of dc source voltage

$$G = \frac{\hat{v}_{\mathrm{ac}}}{V_{\mathrm{dc}}/2} = B \cdot M_i \tag{6}$$

in which

$$B = \frac{1}{1 - 2d_{\mathrm{ST}}} \tag{7}$$

where M_i is the modulation index, and B is the boost factor determined by ST duty ratio d_{ST}.

The obtainable d_{ST} increases with the decrease of M_i. As described by Shen et al. [17], d_{ST} and M_i meet

$$d_{\mathrm{ST}} = 1 - M_i \quad (0 \leq M_i \leq 1) \quad \text{for SCPWM} \tag{8}$$

$$d_{\mathrm{ST}} = 1 - \frac{\sqrt{3}}{2}M_i \quad (0 \leq M_i \leq \frac{2}{\sqrt{3}}) \text{ for MCPWM} \tag{9}$$

$$d_{\mathrm{ST}}(\omega t) = 1 - \frac{\sqrt{3}}{2}M_i \cos\left(\omega t - \frac{\pi}{6}\right) \quad \left(0 \leq \omega t \leq \frac{\pi}{3},\right.$$

$$\left. 0 \leq M_i \leq \frac{2}{\sqrt{3}}\right) \quad \text{for MPWM.} \tag{10}$$

A. SCPWM + 1P ST and MCPWM + 1P ST

Fig. 5 shows the equivalent carrier wave based PWM and the switching state for MCPWM + 1P ST. The ST interval is divided into six parts and averagely inserted in each phase by overlapping the upper and lower switches at every switching commutation. The control reference of six switches for Z-source
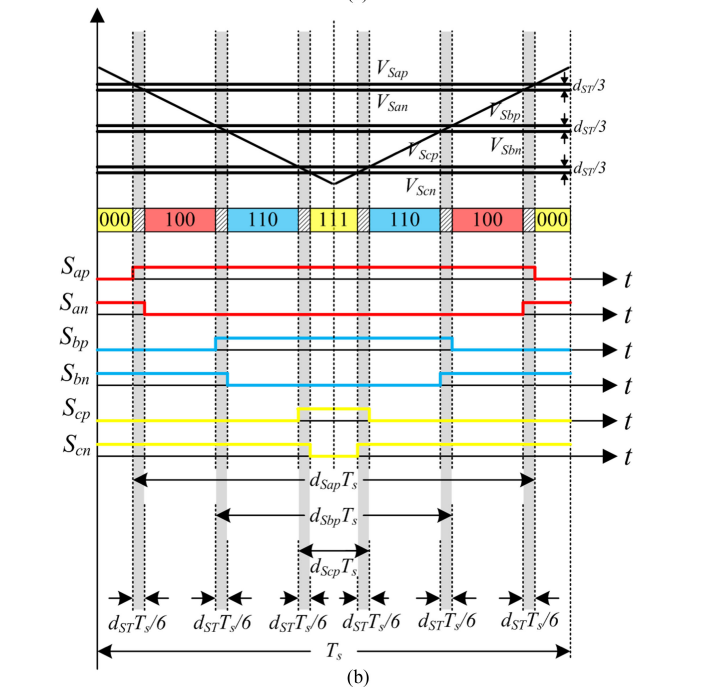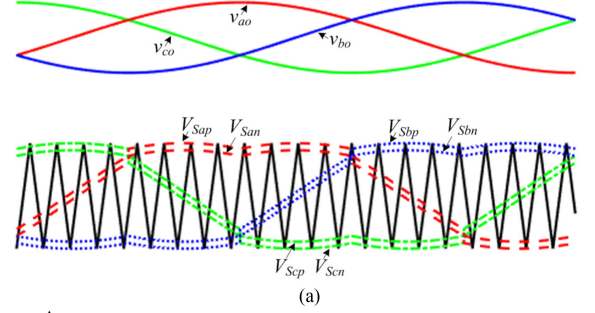

Fig. 5.   MCPWM with 1P ST (MCPWM + 1P ST). (a) Equivalent carrier wave based PWM. (b) Switching states in the first sextant ($0 \leq \omega t \leq \pi/3$).

inverter can be obtained as (11) by shifting the modulation waveforms of conventional three-phase VSI [19]. $V_{\max}^*$, V_{mid}^*, and $V_{\min}^*$ refer to the modulation waveform of conventional three-phase VSI. Take the first sextant, for example, the output voltage meets $v_{\mathrm{ao}} > v_{\mathrm{bo}} > v_{\mathrm{co}}$, so $V_{\max}^* = V_{\mathrm{Sap(San)}}^*$, $V_{\mathrm{mid}}^* = V_{\mathrm{Sbp(Sbn)}}^*$, and $V_{\min}^* = V_{\mathrm{Scp(Scn)}}^*$ in (4) or (5). $V_{\mathrm{Sap}} = V_{\max\_Sp}$, $V_{\mathrm{San}} = V_{\max\_Sn}$, $V_{\mathrm{Sbp}} = V_{\mathrm{mid}\_Sp}$, $V_{\mathrm{Sbn}} = V_{\mathrm{mid}\_Sn}$, $V_{\mathrm{Scp}} = V_{\min\_Sp}$, and $V_{\mathrm{Scn}} = V_{\min\_Sn}$ are the modified modulation waveform expressions for MCPWM + 1P ST in Fig. 5

$$\begin{cases} V_{\max\_Sp}(\omega t) = V_{\max}^*(\omega t) + \dfrac{1}{2}d_{\mathrm{ST}}(\omega t) \\[2mm] V_{\max\_Sn}(\omega t) = V_{\max}^*(\omega t) + \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm] V_{\mathrm{mid}\_Sp}(\omega t) = V_{\mathrm{mid}}^*(\omega t) + \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm] V_{\mathrm{mid}\_Sn}(\omega t) = V_{\mathrm{mid}}^*(\omega t) - \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm] V_{\min\_Sp}(\omega t) = V_{\min}^*(\omega t) - \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm] V_{\min\_Sn}(\omega t) = V_{\min}^*(\omega t) - \dfrac{1}{2}d_{\mathrm{ST}}(\omega t) \end{cases} \tag{11}$$

Fig. 6. MCPWM with 3P ST (MCPWM + 3P ST). (a) Equivalent carrier wave based PWM. (b) Switching states in the first sextant $(0 \leq \omega t \leq \pi/3)$.

where the subscript max, mid, and min refer to the phase of maximum, middle, and minimum output voltage.

B. SCPWM + 3P ST and MCPWM + 3P ST

Fig. 6 shows the equivalent carrier wave based PWM and the switching state for MCPWM + 3P ST. 3P ST method inserts ST interval in three-phase legs to replace zero state. The instantaneous ST current is averagely distributed among three-phase legs, which is beneficial to reduce the current stress and conduction loss of power devices. However, it introduces an additional switching commutation. As shown in Fig. 6, two straight lines $V_{\mathrm{ST\_up}}$ and $V_{\mathrm{ST\_low}}$ compared with triangular waveform are adopted to control ST interval [17]. During non-ST interval, control references of six switches for Z-source inverter are the same as modulation waveforms of conventional VSI expressed in (5) in the first sextant

$$
\begin{cases}
V_{\mathrm{ST\_up}}(\omega t) = 1 - \dfrac{1}{2}d_{\mathrm{ST}}(\omega t) \\[2mm]
V_{\mathrm{max\_Sp(Sn)}}(\omega t) = V_{\max}^*(\omega t) \\
V_{\mathrm{mid\_Sp(Sn)}}(\omega t) = V_{\mathrm{mid}}^*(\omega t) \\
V_{\mathrm{min\_Sp(Sn)}}(\omega t) = V_{\min}^*(\omega t) \\[2mm]
V_{\mathrm{ST\_low}}(\omega t) = \dfrac{1}{2}d_{\mathrm{ST}}(\omega t)
\end{cases}
\tag{12}
$$

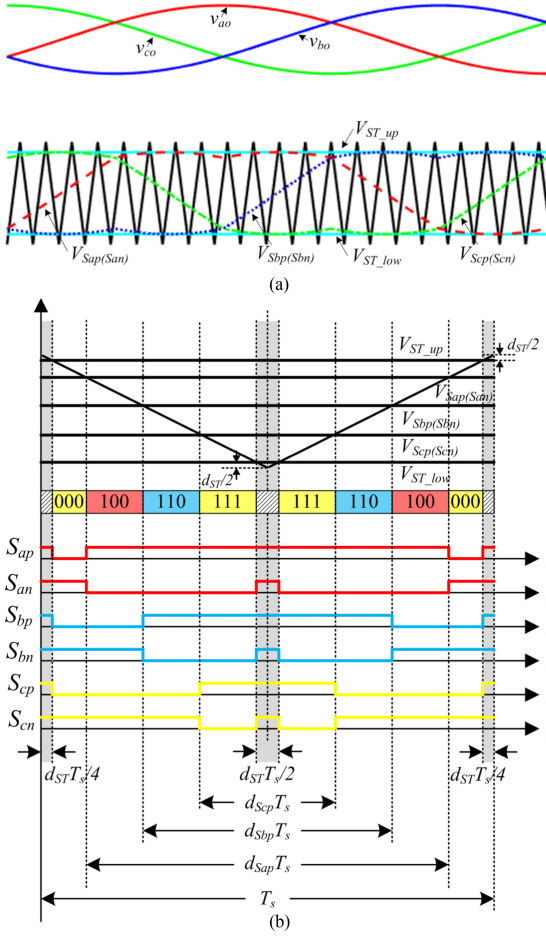Fig. 7. MPWM with 1P ST (MPWM + 1P ST). (a) Equivalent carrier wave based PWM. (b) Switching states in the first sextant $(0 \leq \omega t \leq \pi/3)$.

C. MPWM + 1P ST

When MPWM is applied, all the zero-state intervals shown in Fig. 4 are used for ST. Thus, from (5), the ST duty ratio in the first sextant can be calculated as (10). And it changes with six-time line frequency. Fig. 7 shows the equivalent carrier wave based PWM and the switching state for MPWM + 1P ST [16], [19]. Substituting (10) into (11), the modulation waveforms of six switches can be rewritten as

$$
\begin{cases}
V_{\mathrm{max\_Sp}}(\omega t) = 1 \\[2mm]
V_{\mathrm{max\_Sn}}(\omega t) = V_{\max}^*(\omega t) + \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm]
V_{\mathrm{mid\_Sp}}(\omega t) = V_{\mathrm{mid}}^*(\omega t) + \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm]
V_{\mathrm{mid\_Sn}}(\omega t) = V_{\mathrm{mid}}^*(\omega t) - \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm]
V_{\mathrm{min\_Sp}}(\omega t) = V_{\min}^*(\omega t) - \dfrac{1}{6}d_{\mathrm{ST}}(\omega t) \\[2mm]
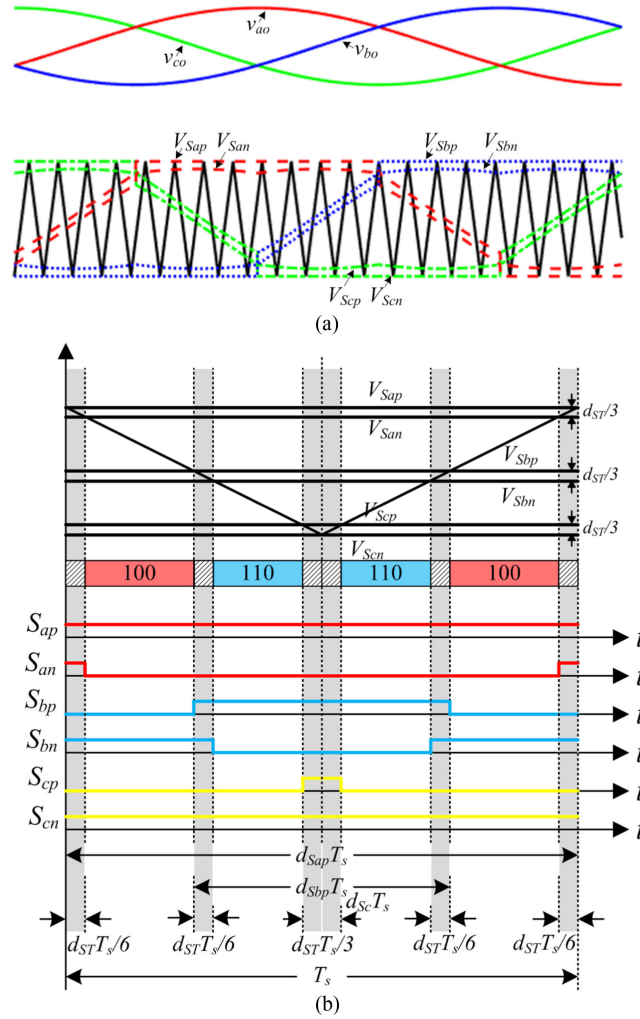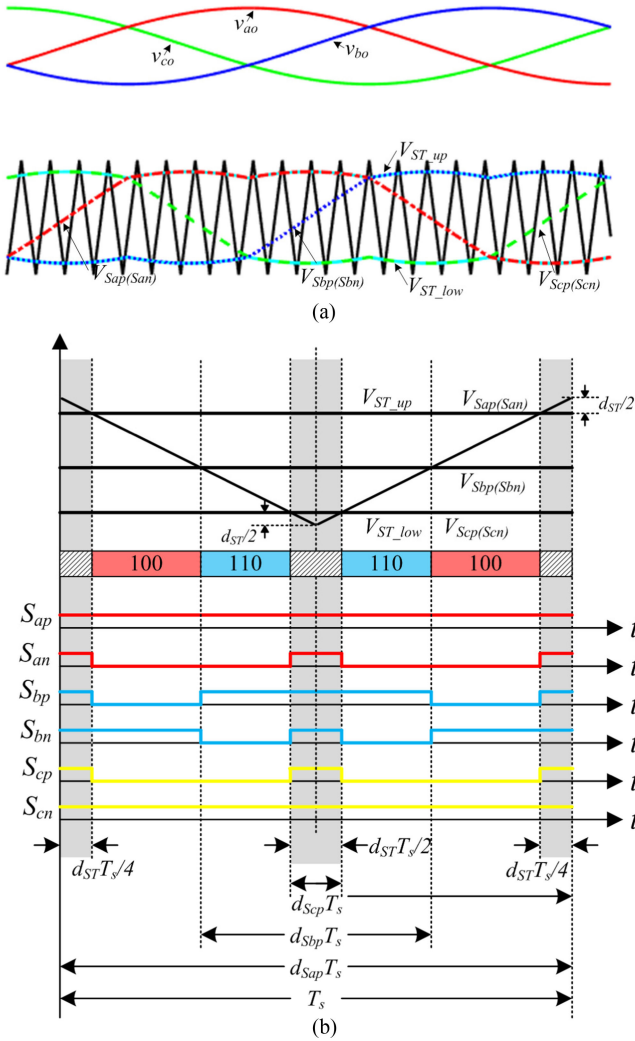V_{\mathrm{min\_Sn}}(\omega t) = 0
\end{cases}
\tag{13}
$$

(a)

(b)

Fig. 8. MPWM with 3P ST (MPWM + 3P ST). (a) Equivalent carrier wave based PWM. (b) Switching states in the first sextant ($0 \leq \omega t \leq \pi/3$).

D. MPWM + 3P ST

Fig. 8 shows the equivalent carrier wave based PWM and the switching state for MPWM + 3P ST. Two curves $V_{\mathrm{ST\_up}}$ and $V_{\mathrm{ST\_low}}$ for ST interval control are the instantaneous maximum and minimum value of three-phase modulation waveforms. The control references of six switches can be written as

$$
\begin{cases}
V_{\mathrm{ST\_up}}(\omega t) = V_{\mathrm{max\_Sp(Sn)}}(\omega t) \\
V_{\mathrm{max\_Sp(Sn)}}(\omega t) = V^*_{\mathrm{max}}(\omega t) \\
V_{\mathrm{mid\_Sp(Sn)}}(\omega t) = V^*_{\mathrm{mid}}(\omega t) \\
V_{\mathrm{min\_Sp(Sn)}}(\omega t) = V^*_{\mathrm{min}}(\omega t) \\
V_{\mathrm{ST\_low}}(\omega t) = V_{\mathrm{min\_Sp(Sn)}}(\omega t)
\end{cases} \qquad (14)
$$

III. IPWM Strategy of Z-Source Inverter

Fig. 9 shows the relationship of three-phase output voltage and available minimum dc-link voltage for conventional three-phase VSI with SPWM and SVM. The fundamental frequency f_{line} is 50 Hz for analysis. Using SPWM, the minimum constant dc-link voltage is twice the peak value of output phase voltage
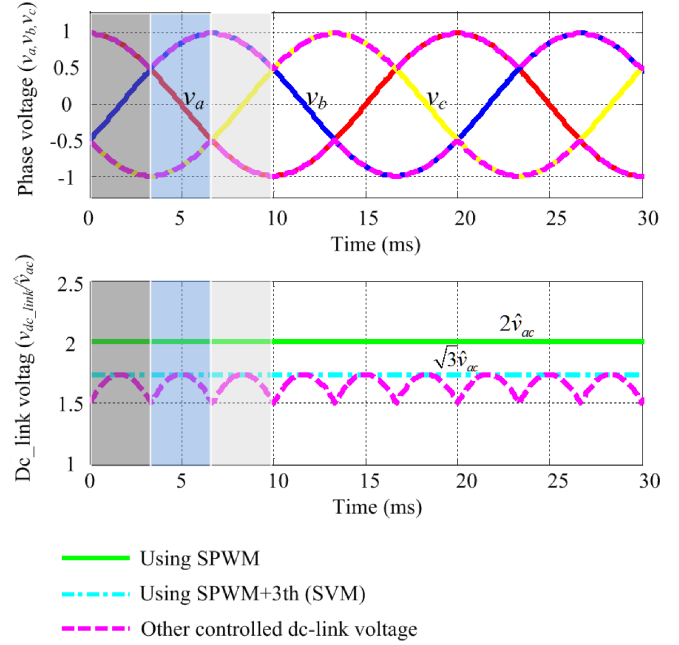

Fig. 9. Available dc-link voltage of the inverter bridge.

$2\hat{v}_{\mathrm{ac}}$, which is represented by the green solid line. Using SPWM with 3rd harmonic injection or SVM to increase dc-link voltage utilization, the minimum constant dc-link voltage is $\sqrt{3}\hat{v}_{\mathrm{ac}}$, which is represented by the blue dot-dash line. Besides, there is another available dc-link voltage, which is represented by the magenta dashed line changing with six-time line frequency. It is actually the instantaneous maximum value of three-phase line voltage and it can be expressed as

$$
v^*_{\mathrm{dc\_link}}(\omega t) = \sqrt{3} \cdot \hat{v}_{\mathrm{ac}} \cdot \cos\left(\theta - \frac{\pi}{6}\right) \qquad (15)
$$

where θ is the remainder of ωt divided by $\pi/3$, $\theta = \omega t \% (\pi/3)$.

If the average dc-link voltage in one switching time period $< v_{\mathrm{dc\_link}} >_{Ts}$ can be accurately controlled as the magenta dashed line shown in Fig. 9, the upper switch in the leg of the maximum phase voltage (v_{max}) and the lower switch in the leg of minimum phase voltage (v_{min}) are always turned ON. The upper and lower switches in the rest phase leg (v_{mid}) are controlled with PWM signal. The switching states of power devices in three-phase legs are listed in Table I. The equivalent switching frequency of power devices can be reduced to $1/3 f_s$ $(f_s = 1/T_s)$. Take the first sextant, for example, the instantaneous dc-link voltage is the line voltage $(v_{\mathrm{ao}} - v_{\mathrm{co}})$. S_{ap} and S_{cn} are always turned ON. S_{bp} and S_{bn} are controlled with PWM to regulate v_{bo}. In each sextant, only one phase leg operates under complementary PWM mode. And the corresponding duty ratio of upper and lower switch $d^*_{\mathrm{Sip}}, d^*_{\mathrm{Sin}}$ are expressed as

$$
\begin{cases}
d^*_{\mathrm{Sip}}(\omega t) = \dfrac{v_{\mathrm{mid}}(\omega t) - v_{\mathrm{min}}(\omega t)}{v_{\mathrm{max}}(\omega t) - v_{\mathrm{min}}(\omega t)} \\
d^*_{\mathrm{Sin}}(\omega t) = 1 - d^*_{\mathrm{Sip}}(\omega t)
\end{cases} \qquad (16)
$$

where in each sextant, $v_{\mathrm{min}}(\omega t) = \min(v_{\mathrm{ao}}, v_{\mathrm{bo}}, v_{\mathrm{co}})$; $v_{\mathrm{max}}(\omega t) = max(v_{\mathrm{ao}}, v_{\mathrm{bo}}, v_{\mathrm{co}})$; $v_{\mathrm{mid}}(\omega t) = \mathrm{mid}(v_{\mathrm{ao}}, v_{\mathrm{bo}}, v_{\mathrm{co}})$;

TABLE I
SWITCHING STATES OF POWER DEVICES IN THE INVERTER BRIDGE

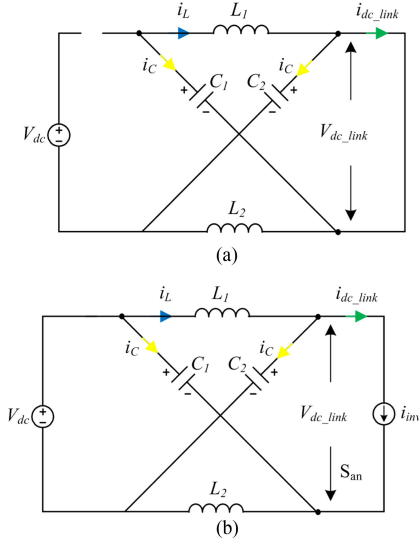| Phase angle	$0° \leq \theta \leq 60°$	$60° \leq \theta \leq 120°$	$120° \leq \theta \leq 180°$	$180° \leq \theta \leq 240°$	$240° \leq \theta \leq 300°$	$300° \leq \theta \leq 360°$
Mod A	$S_{\mathrm{ap}} = 1; S_{\mathrm{an}} = 0$	$S_{\mathrm{ap}} S_{\mathrm{an}} = \mathrm{PWM}$	$S_{\mathrm{ap}} = 0; S_{\mathrm{an}} = 1$	$S_{\mathrm{ap}} = 0; S_{\mathrm{an}} = 1$	$S_{\mathrm{ap}} S_{\mathrm{an}} = \mathrm{PWM}$	$S_{\mathrm{ap}} = 1; S_{\mathrm{an}} = 0$
Mod B	$S_{\mathrm{bp}} S_{\mathrm{bn}} = \mathrm{PWM}$	$S_{\mathrm{bp}} = 1; S_{\mathrm{bn}} = 0$	$S_{\mathrm{bp}} = 1; S_{\mathrm{bn}} = 0$	$S_{\mathrm{bp}} S_{\mathrm{bn}} = \mathrm{PWM}$	$S_{\mathrm{bp}} = 0; S_{\mathrm{bn}} = 1$	$S_{\mathrm{bp}} = 0; S_{\mathrm{bn}} = 1$
Mod C	$S_{\mathrm{cp}} = 0; S_{\mathrm{cn}} = 1$	$S_{\mathrm{cp}} = 0; S_{\mathrm{cn}} = 1$	$S_{\mathrm{cp}} S_{\mathrm{cn}} = \mathrm{PWM}$	$S_{\mathrm{cp}} = 1; S_{\mathrm{cn}} = 0$	$S_{\mathrm{cp}} = 1; S_{\mathrm{cn}} = 0$	$S_{\mathrm{cp}} S_{\mathrm{cn}} = \mathrm{PWM}$

Fig. 10. Equivalent circuit of Z-source inverter viewed from the dc-link of the inverter bridge. (a) During ST interval. (b) During non-ST interval.

and i representing the phase of $v_{\mathrm{mid}}(\omega t)$ changes between a, b, and c.

As for conventional two-stage buck–boost VSI, at the intermediate dc link, there is a large aluminum electrolytic capacitor to absorb the high frequency current harmonics and compensate the transient power difference between the front boost circuit and inverter bridge [32]. Usually, the intermediate dc-link voltage is kept almost constant by adjusting the boost duty ratio in steady state. It is difficult or even impossible to control the intermediate dc-link voltage like a six-pulse waveform. However, for Z-source inverter, $v_{\mathrm{dc\_link}}$ is chopped dc voltage with high switching frequency. Therefore, maybe there is a new PWM strategy that is suitable for Z-source inverter.

According to the operation principles of Z-source inverter described in Peng [3], Fig. 10 shows two equivalent circuits seen from the dc link of the inverter bridge. During ST interval, D_0 is reverse biased and Z-source network is shorted $v_{\mathrm{dc\_link}} = 0$. During non-ST interval, D_0 is conducting, both capacitors and dc source are reversely connected to supply the inverter bridge $v_{\mathrm{dc\_link}} = 2V_C - V_{\mathrm{dc}}$. Thus, the average intermediate dc-link voltage in one switching time period is calculated in the following equation:

$$< v_{\mathrm{dc\_link}} >_{T_s} = \frac{1}{T_s} \cdot \left(\int_0^{d_{\mathrm{ST}} \cdot T_s} 0 \, dt + \int_{d_{\mathrm{ST}} \cdot T_s}^{T_s} (2V_C - V_{\mathrm{dc}}) \, dt \right)$$
$$= (1 - d_{\mathrm{ST}}) \cdot (2V_C - V_{\mathrm{dc}}). \quad (17)$$

From (17), $< v_{\mathrm{dc\_link}} >_{T_s}$ can be regulated intermediately by adjusting d_{ST}. For simple analysis, it is assumed that the

capacitance of C_1 and C_2 is large enough and the voltage is almost constant in steady state. In order to reduce the switching frequency of power devices in the inverter bridge so that a higher efficiency can be attained, it is possible to regulate $< v_{\mathrm{dc\_link}} >_{T_s}$ to meet (15). Obviously, d_{ST} is periodically changing in every 60° (1/6 output line frequency period)

$$(1 - d_{\mathrm{ST}}(\omega t)) \cdot (2V_C - V_{\mathrm{dc}}) = \sqrt{3} \cdot \hat{v}_{\mathrm{ac}} \cdot \cos\left(\theta - \frac{\pi}{6}\right) \quad (18)$$

where θ is the remainder of ωt divided by $\pi/3$, $\theta = \omega t \% (\pi/3)$.

In this case, the average voltage of inductor in one sextant should be zero, according to volt-second balance principle

$$\frac{3}{\pi} \int_0^{\pi/3} (d_{\mathrm{ST}}(\omega t) T_s \cdot V_C + (1 - d_{\mathrm{ST}}(\omega t)) T_s$$
$$\cdot (V_{\mathrm{dc}} - V_C)) \, d\omega t = 0. \quad (19)$$

Ignoring the low frequency ripples associated with output line frequency f_{line}, V_C is determined by the average value of ST duty ratio d_{avg}

$$V_C = \frac{1 - \frac{3}{\pi} \int_0^{\pi/3} d_{\mathrm{ST}}(\omega t) d\omega t}{1 - 2 \cdot \frac{3}{\pi} \int_0^{\pi/3} d_{\mathrm{ST}}(\omega t) d\omega t} V_{\mathrm{dc}} = \frac{(1 - d_{\mathrm{avg}}) V_{\mathrm{dc}}}{1 - 2d_{\mathrm{avg}}} \quad (20)$$

in which, d_{avg} can be calculated by integrating $d_{\mathrm{ST}}(\omega t)$ in (18) in one sextant

$$d_{\mathrm{avg}} = \frac{3}{\pi} \cdot \int_0^{\pi/3} \left(1 - \frac{v_{\mathrm{dc\_link}}(\omega t)}{2V_C - V_{\mathrm{dc}}} \right) \cdot d\omega t$$
$$= 1 - \frac{3\sqrt{3}}{\pi} \cdot \frac{\hat{v}_{\mathrm{ac}}}{2V_C - V_{\mathrm{dc}}}. \quad (21)$$

Solving (6), (20), and (21), the capacitor voltage in steady state can be derived as

$$V_C = \frac{3\sqrt{3}G}{2\pi} \cdot V_{\mathrm{dc}}. \quad (22)$$

And the ST duty ratio is

$$d_{\mathrm{ST}}(\omega t) = 1 - \frac{\pi}{3}(1 - d_{\mathrm{avg}}) \cos\left(\omega t - \frac{\pi}{6}\right) \quad (23)$$

$$d_{\mathrm{avg}} = \frac{3\sqrt{3}G - 2\pi}{6\sqrt{3}G - 2\pi}. \quad (24)$$

When Z-source inverter operates under boost mode, $d_{\mathrm{ST}}(\omega t) \geq 0$. So G should be larger than 1.27 from (23) and (24).

Fig. 11 shows the switching state of IPWM strategy for Z-source inverter in the first sextant. The ST interval is symmetrically inserted into the phase-leg of v_{mid}. In the first sextant, the output three-phase voltage meet $v_{\mathrm{max}} = v_{\mathrm{ao}}$, $v_{\mathrm{mid}} = v_{\mathrm{bo}}$, and $v_{\mathrm{min}} = v_{\mathrm{co}}$. The thick-shaded part represents the ST
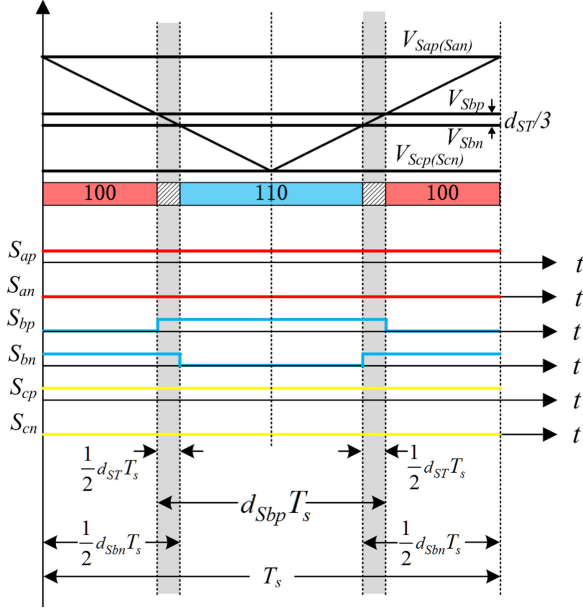
Fig. 11.   Switching states of Z-source inverter with IPWM strategy in the first sextant.

Fig. 12.   Equivalent carrier waveform based PWM for IPWM + 1P ST.

interval, which serves to regulate the intermediate dc-link voltage ($< v_{\mathrm{dc\_link}}>_{T_s} = v_{\mathrm{ao}} - v_{\mathrm{co}}$). The active voltage vectors (110, 100) are implemented during non-ST interval to regulate v_{bo}. For symmetry, the switching states in other sextants can be obtained similarly. Since only power devices in one phase leg operate at high switching frequency, IPWM + 1P ST can minimize the equivalent switching frequency of power devices in the inverter bridge. As a result, it can be predicted that the switching loss will be reduced to a great extent. As shown in Fig. 11, according to volt-second balance principle, the duty ratio of upper switch d_{Sip} and lower switch d_{Sin}, output voltage of phase B v_{mid} meets

$$\begin{cases} v_{\mathrm{mid}}(\omega t) - v_{\mathrm{min}}(\omega t) = (d_{\mathrm{Sbp}}(\omega t) - d_{\mathrm{ST}}(\omega t)) \cdot (2V_C - V_{\mathrm{dc}}) \\ d_{\mathrm{Sbn}}(\omega t) = 1 - d_{\mathrm{Sbp}}(\omega t) + d_{\mathrm{ST}}(\omega t). \end{cases}$$
(25)

Furthermore, $< v_{\mathrm{dc\_link}} >_{Ts}$ is controlled the same as maximum value of three-phase line voltage

$$(1 - d_{\mathrm{ST}}(\omega t)) \cdot (2V_C - V_{\mathrm{dc}}) = v_{\mathrm{max}}(\omega t) - v_{\mathrm{min}}(\omega t). \quad (26)$$

Combining (24)–(26), the corresponding duty ratio expressions of the upper and lower switches d_{Sip} and d_{Sin} in (16) can be modified as

$$\begin{cases} d_{\mathrm{Sip}}(\omega t) = \dfrac{v_i(\omega t) - v_{\mathrm{min}}(\omega t)}{v_{\mathrm{max}}(\omega t) - v_{\mathrm{min}}(\omega t)} \cdot (1 - d_{\mathrm{ST}}(\omega t)) + d_{\mathrm{ST}}(\omega t) \\ d_{\mathrm{Sin}}(\omega t) = 1 - d_{\mathrm{Sip}}(\omega t) + d_{\mathrm{ST}}(\omega t). \end{cases}$$
(27)

Like the typical PWM strategies of Z-source inverter, IPWM + 1P ST can be obtained by the level shift of conventional three-phase VSI modulation waveforms. Fig. 12 shows the equivalent carrier wave based PWM and switching state for IPWM + 1P ST. Six modulation waveforms are compared with the triangular wave to produce the gate signals for switches in
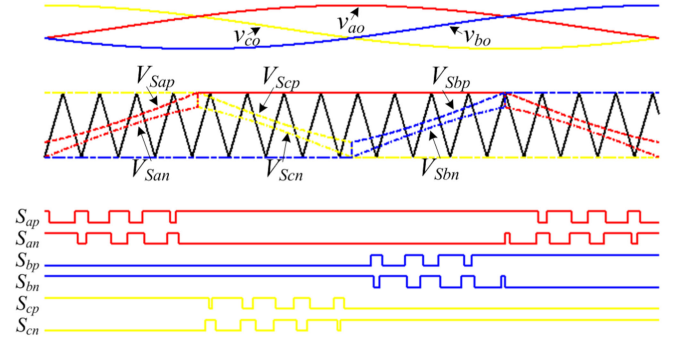
Z-source inverter. Assume the amplitude of triangular wave is normalized, the modulation waveform expressions of six switches are expressed as follows:

$$\begin{cases} V_{\mathrm{max\_Sp}}(\omega t) = V_{\mathrm{max\_Sn}}(\omega t) = 1 \\ V_{\mathrm{mid\_Sp}}(\omega t) = V_{\mathrm{mid}}^{*}(\omega t) + \dfrac{1}{2}d_{\mathrm{ST}}(\omega t) \\ V_{\mathrm{mid\_Sn}}(\omega t) = V_{\mathrm{mid}}^{*}(\omega t) - \dfrac{1}{2}d_{\mathrm{ST}}(\omega t) \\ V_{\mathrm{min\_Sp}}(\omega t) = V_{\mathrm{min\_Sn}}(\omega t) = 0 \end{cases}$$
(28)

where V_{mid}^{*} refer to the modulation of conventional three-phase VSI in (5).

IV. COMPARISON OF PWM STRATEGIES

To investigate the inherent advantages and disadvantages of IPWM + 1P ST, comparisons with the typical PWM strategies are carried out in terms of voltage boost capability, the requirements of power devices and passive components. According to the operation principle of Z-source inverter using different PWM strategies, the steady-state operation points including voltage gain G, ST interval d_{ST}, capacitor voltage V_C, and inductor current I_L can be derived and listed in Table II. The voltage gain comparison of Z-source inverter with different PWM strategies is shown in Fig. 13. Due to full utilization of intermediate dc-link voltage, IPWM + 1P ST and MPWM + 1P/3P ST have the maximum voltage boost capability.

A. Power Devices Comparison

As for Z-source inverter using SCPWM + 1P ST and MCPWM + 1P ST shown in Fig. 5, the switching frequency of power devices in the inverter bridge and D_0 are f_s and $6f_s$ ($f_s = 1/T_s$), respectively. For Z-source inverter using MPWM + 1P ST shown in Fig. 7, the switching frequency of power devices in the inverter bridge and D_0 are $2/3f_s$ and $4f_s$, respectively. IPWM + 1P ST uses single-phase leg for ST current conduction without introducing an additional switching commutation, which is different from the existing PWM strategies. The equivalent switching frequency is reduced to $1/3f_s$, which is the minimum value among the existing PWM strategies. Table III lists the equivalent switching frequency of power devices for Z-source inverter with different PWM strategies ($f_s = 1/T_s$).

TABLE II
EXPRESSIONS OF VOLTAGE GAIN FOR Z-SOURCE INVERTER WITH DIFFERENT PWM STRATEGIES

| Modulation scheme	SCPWM + 1P ST [3], SCPWM + 3P ST [3],	MCPWM + 1P ST [17], MCPWM + 3P ST [17],	MPWM + 1P ST [16] MPWM + 3P ST [16] IPWM + 1P ST
Voltage gain(G)	$G = \frac{1-d_{ST}}{1-2d_{ST}} = \frac{M_i}{2M_i-1}$	$G = \frac{2}{\sqrt{3}}\frac{1-d_{ST}}{1-2d_{ST}} = \frac{M_i}{\sqrt{3}M_i-1}$	$G = \frac{2\pi}{3\sqrt{3}}\frac{1-d_{avg}}{1-2d_{avg}} = \frac{\pi M_i}{3\sqrt{3}M_i-\pi}$
ST interval(d_{ST} or d_{avg})	$d_{ST} = 1 - M_i = \frac{G-1}{2G-1}$	$d_{ST} = 1 - \frac{\sqrt{3}}{2}M_i = \frac{\sqrt{3}G-2}{2\sqrt{3}G-2}$	$d_{avg} = 1 - \frac{3\sqrt{3}}{2\pi}M_i = \frac{3\sqrt{3}G-2\pi}{6\sqrt{3}G-2\pi}$
Modulation index (M_i)	$M_i = 1 - d_{ST} = \frac{G}{2G-1}$	$M_i = \frac{2}{\sqrt{3}}(1-d_{ST}) = \frac{G}{\sqrt{3}G-1}$	$M_i = \frac{2\pi}{3\sqrt{3}}(1-d_{avg}) = \frac{\pi G}{3\sqrt{3}G-\pi}$
Capacitor voltage(V_C)	$V_C = \frac{1-d_{ST}}{1-2d_{ST}}V_{dc} = GV_{dc}$	$V_C = \frac{1-d_{ST}}{1-2d_{ST}}V_{dc} = \frac{\sqrt{3}G}{2}V_{dc}$	$V_C = \frac{1-d_{avg}}{1-2d_{avg}}V_{dc} = \frac{3\sqrt{3}G}{2\pi}V_{dc}$
Inductor current(I_L)	$i_L = \frac{3}{4}G\hat{i}_{ac} = \frac{3}{4}\frac{1-d_{ST}}{1-2d_{ST}}\hat{i}_{ac}$	$i_L = \frac{3}{4}G\hat{i}_{ac} = \frac{3}{2\sqrt{3}}\frac{1-d_{ST}}{1-2d_{ST}}\hat{i}_{ac}$	$i_L = \frac{3}{4}G\hat{i}_{ac} = \frac{\pi}{2\sqrt{3}}\frac{1-d_{avg}}{1-2d_{avg}}\hat{i}_{ac}$
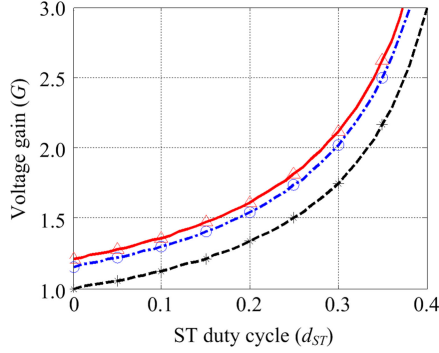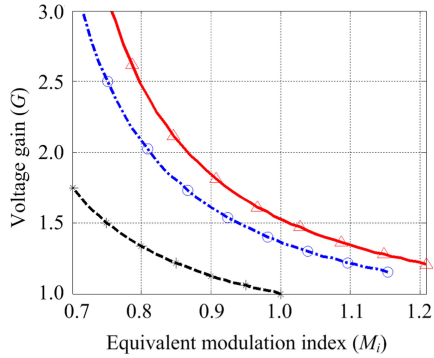
Fig. 13. Voltage gain of Z-source inverter with different modulation strategies. (a) G and d_{ST}. (b) G and M_i.

TABLE III
EQUIVALENT SWITCHING FREQUENCY OF POWER DEVICES FOR Z-SOURCE INVERTER WITH DIFFERENT PWM STRATEGIES ($f_s = 1/T_s$)

Modulation scheme	Switching frequency	
	Front diode	Switches in inverter bridge
SCPWM + 3P ST, MCPWM + 3P ST [17]	$2f_s$	$2f_s$
SCPWM + 1P ST, MCPWM + 1P ST [17]	$6f_s$	f_s
MPWM + 3P ST [16]	$2f_s$	$4f_s/3$
MPWM+ 1P ST [16]	$4f_s$	$2f_s/3$
IPWM + 1P ST	$2f_s$	$f_s/3$
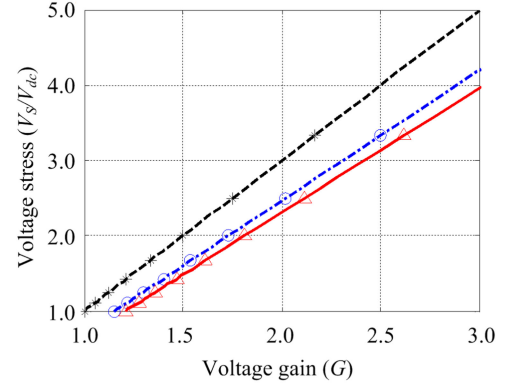
Fig. 14. Voltage stress of power device for Z-source inverter with different PWM strategies.

According to the operation principle of Z-source inverter, D_0 and switching devices in the inverter bridge withstand the same voltage stress, which is the maximum of intermediate dc-link voltage in the following equation:

$$v_s = 2V_C - V_{dc}. \qquad (29)$$

For existing PWM strategies and IPWM, substituting V_C listed in Table II into (29), the voltage stress of power devices as function of voltage gain G can be derived as follows:

$$v_s = (2G - 1)V_{dc} \quad \text{(SCPWM + 1P/3P ST)} \qquad (30)$$

$$v_s = \frac{\sqrt{3}G - 2}{2}V_{dc} \quad \text{(MCPWM + 1P/3P ST)} \qquad (31)$$

$$v_s = \frac{3\sqrt{3}G - 2\pi}{2\pi}V_{dc}$$

$$\text{(MPWM + 1P/3P ST or IPWM + 1P ST).} \qquad (32)$$

Fig. 14 shows the power devices voltage stress comparison for Z-source inverter with different PWM strategies. MPWM strategies (IPWM + 1P ST and MPWM + 1P/3P ST) have the minimum voltage stress of power devices.

In addition to voltage stress, another key parameter for the selection of power device is the current stress (I_S). The three typical indicators reflecting power device current stress are as follows:
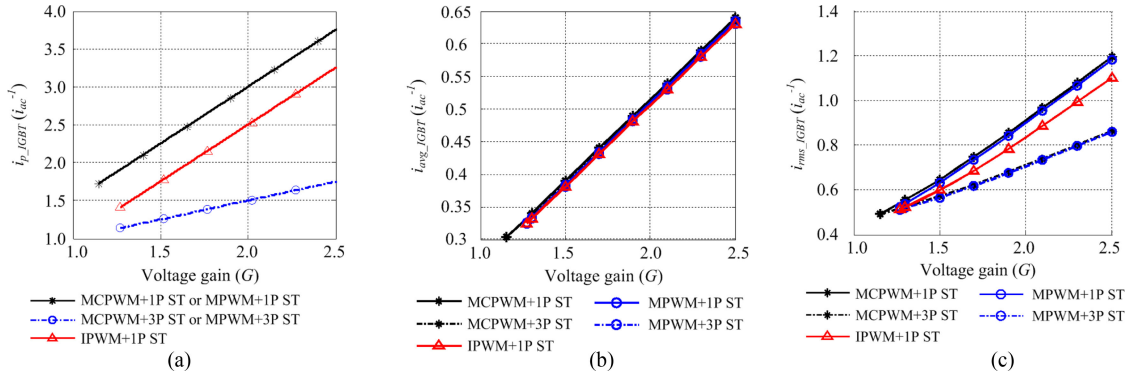
Fig. 15.   Current stress of insulated-gate bipolar transistor (IGBT) $(\cos(\varphi) = 1)$. (a) i_{p_IGBT}. (b) i_{avg_IGBT}. (c) i_{rms_IGBT}.
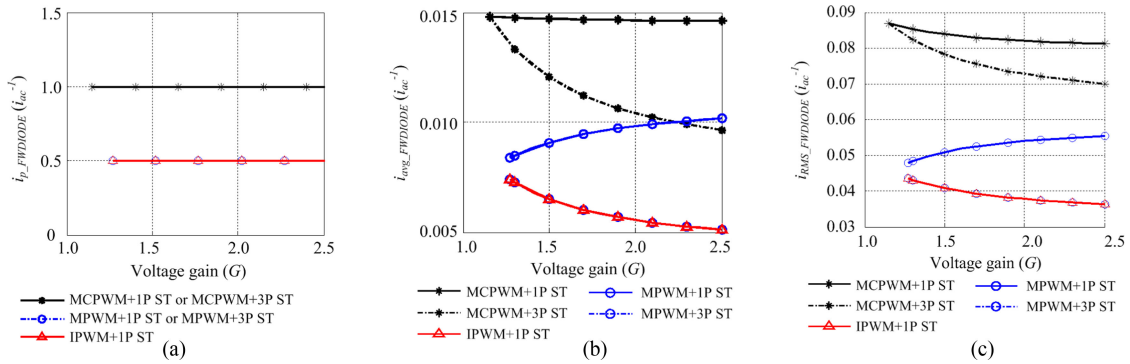

Fig. 16.   Current stress of free-wheeling diode $(\cos(\varphi) = 1)$. (a) $i_{p\_FWDIODE}$. (b) $i_{avg\_FWDIODE}$. (c) $i_{rms\_FWDIODE}$.

1) I_{S_peak}, the maximum instant current flowing through the power device defined as (33);
2) I_{S_avg}, the average current flowing through power device in each output line-frequency period defined as (34);
3) I_{S_rms}, the root mean square (rms) value of current flowing through power device in each output line-frequency period defined as (35) [32]

$$I_{S\_peak} = \max(i_S(\omega t)) \tag{33}$$

$$I_{S\_avg} = \frac{1}{2\pi} \left[\begin{array}{l} \int_0^{2\pi} d_{ST}(\omega t) \cdot i_{S\_ST}(\omega t) d(\omega t) \\ + \int_0^{2\pi} d_{NST}(\omega t) \cdot i_{S\_NST}(\omega t) d(\omega t) \end{array} \right] \tag{34}$$

$$I_{S\_rms} = \sqrt{\frac{1}{2\pi} \left[\begin{array}{l} \int_0^{2\pi} d_{ST}(\omega t) \cdot i_{ST}^2(\omega t) d(\omega t) \\ + \int_0^{2\pi} d_{NST}(\omega t) \cdot i_{NST}^2(\omega t) d(\omega t) \end{array} \right]} \tag{35}$$

According to the definition in (33)–(35), the average and rms current calculation depends on the on-state duty ratio and current across power device. The mathematic expressions of on-state duty ratio and on-state current in different switching states are derived in the Appendix. Then, it is easier to use numerical calculation to get the comparison results.

Figs. 15–17 show the current stress of insulated-gate bipolar transistor (IGBT), free-wheeling diode, and D_0 for Z-source inverter with different PWM strategies, respectively. The load power factor is unit 1 here $(\cos(\varphi) = 1)$. As shown in Fig. 15(a), MCPWM + 3P ST and MPWM + 3P ST have the minimum peak current. It is because the large ST current is simultaneously distributed among three-phase legs. Compared with MCPWM + 1P ST and MPWM + 1P ST, IPWM + 1P ST is beneficial to reduce IGBT peak current. This is because the ST interval is inserted in the phase of v_{mid}. As shown in Fig. 15(b), all these PWM strategies have almost the same average current stress of IGBT. This is because eventually the ST current is averagely distributed among three-phase legs in each output line-frequency period. $(T_{line} = 1/f_{line})$. When it comes to rms current of IGBT, PWM with 3P ST (MCPWM + 3P ST, MPWM + 3P ST) have the minimum value compared to those with 1P ST (MCPWM + 1P ST, MPWM + 1P ST, IPWM + 1P ST). IPWM + 1P ST has a little smaller value of rms current than that of MCPWM + 1P ST, MPWM + 1P ST.

As shown in Fig. 16(a), with MPWM strategies (MPWM + 1P/3P ST, IPWM + 1P ST), free-wheeling diode has the minimum peak current, which is half of MCPWM (MCPWM+1P/3P ST). With MPWM+3P ST and IPWM+1P ST, free-wheeling diode has the minimum average current and RMS current shown in Fig. 16(b) and Fig. 16(c). Under the high load power factor, the average and RMS current of free-wheeling diode are far smaller than that of IGBT.

As shown in Fig. 17, MPWM strategies (MPWM + 1P/3P ST, IPWM + 1P ST) have the minimum value of peak current for D_0. With different PWM strategies, the average current flowing through D_0 is the input current under certain output power. Thus, they have the same value of average current shown in Fig. 17(b). Compared with MCPWM strategies (MCPWM + 1P/3P ST),
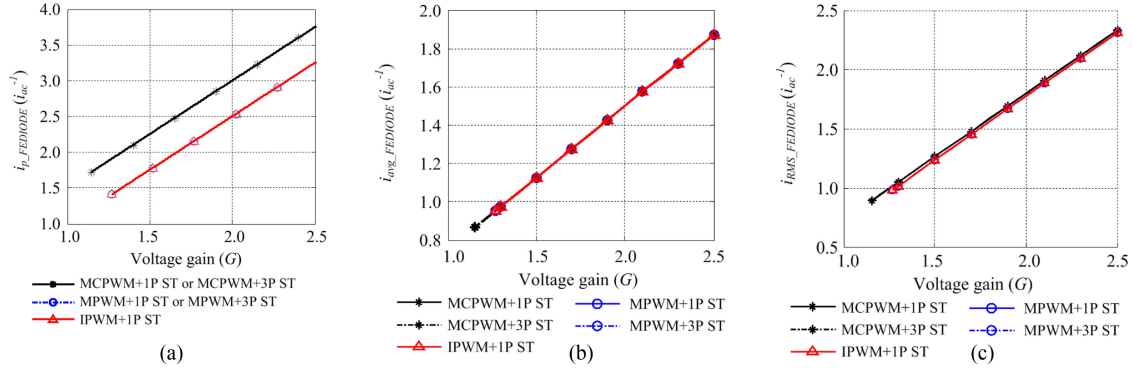
Fig. 17. Current stress of front-end diode $(\cos(\varphi) = 1)$. (a) i_{p_FEDIODE}. (b) $i_{\text{avg\_FEDIODE}}$. (c) $i_{\text{rms\_FEDIODE}}$.

MPWM strategies (MPWM + 1P/3P ST, IPWM + 1P ST) have a little smaller value of rms current.

In all, for Z-source inverter, PWM strategies with different ST injection methods mainly affect the current stress of IGBT, but have little influence on the average and rms current of free-wheeling diode and the front-end diode. Z-source inverter with IPWM + 1P ST demonstrates the maximum voltage boost capability, minimum voltage stress, and minimum switching frequency of power devices.

B. Passive Components Requirement Comparison

In general, the cost and volume of passive component are proportional to the available energy stored in it. The inductor core and winding are designed on the basis of the inductance requirement (L) and average current level (I_L) under maximum operation conditions. The inductance is selected to limit the current ripples in a certain range. The capacitor is designed based on the current capacity, capacitance requirement, and terminal voltage [27]. The current capacity usually refers to the rms value of the current ripples, which is related the capacitor working temperature and service life. The capacitance is selected according to the limitations of the voltage ripple. The current/voltage ripples of inductor/capacitor are defined as

$$\Delta I_L = \delta_L \cdot I_L \tag{36}$$

$$\Delta V_C = \delta_C \cdot V_C \tag{37}$$

where δ_L and δ_C are the ripples coefficients preset based on the performance indices of power converter.

As for MCPWM (MCPWM + 1P/3P ST), d_{ST} in one switching time period is constant. Thus, in theory, passive components just contain switching-frequency ripples, which are analyzed in one switching time period T_s. I_L increases during ST interval and decreases during non-ST interval, whereas v_C decreases during ST interval and increases during non-ST interval.

With MPWM strategies (MPWM + 1P/3P ST, IPWM + 1P ST), d_{ST} expressed in (23) keeps changing in each sextant. The typical waveforms of inductor current and capacitor voltage are shown in Fig. 18, in which, $< v_L >_{Ts}$ is the average value of inductor terminal voltage in one switching time period, and $< i_C >_{Ts}$ is the average value of capacitor current in one switching time period. In theory, besides the switching frequency ripples, the passive components also
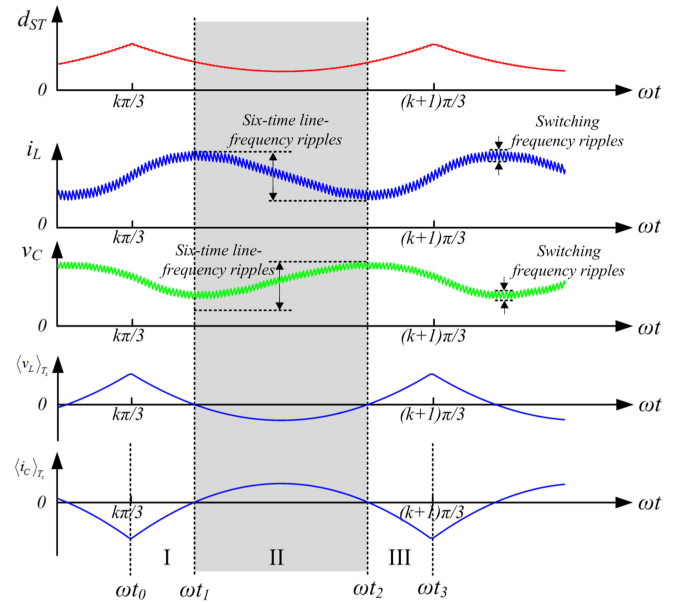
Fig. 18. Inductor current and capacitor voltage waveforms for Z-source inverter with MPWM strategies (MPWM + 1P/3P ST or IPWM + 1P ST).

contain six-time-line-frequency ripples, which are analyzed in one sextant. Usually, the amplitude of switching frequency ripples is much smaller than that of six-time-line-frequency ripples. Thus, the inductance and capacitance in Z-source network should be designed to limit the low-frequency ripples in the desired range. As shown in Fig. 18, i_L increases and v_C decreases during interval II (ωt_1, ωt_2). According to inductor's V–I characteristic, ΔI_L can be calculated by integrating $< v_L >_{Ts}$ from ωt_1 to ωt_2. Similarly, Δv_C can be derived by integrating $< i_C >_{Ts}$ from ωt_1 to ωt_2. The detailed derivation process is in the Appendix. Table IV lists the expressions of inductance and capacitance requirement for Z-source inverter with different PWM strategies.

For Z-source inverter with the different PWM strategies, the current of capacitor keeps changing periodically in every sextant. Thus, the rms current of capacitor can be calculated by integrating i_C in 60°. The expressions of duty ratio and capacitor current in different switching states are derived in the

TABLE IV
EXPRESSIONS OF PASSIVE COMPONENTS REQUIREMENT FOR Z-SOURCE
INVERTER WITH DIFFERENT PWM STRATEGIES

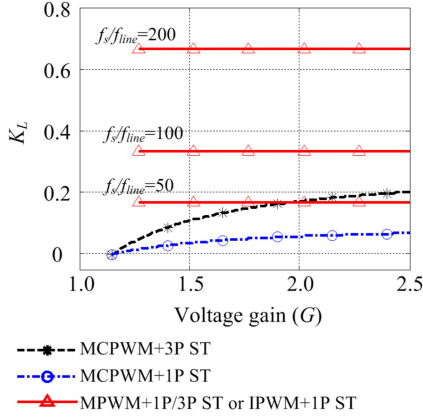| Modulation scheme	Inductance (L)	Capacitance (C)
MCPWM + 3P ST [17]	$L = \frac{1}{2\sqrt{3}} \cdot \frac{\sqrt{3}G-2}{\sqrt{3}G-1} \cdot \frac{V_{\mathrm{dc}}}{\delta_L \cdot f_s \cdot \hat{i}_{\mathrm{ac}}}$	$C = \frac{\sqrt{3}}{8} \cdot \frac{\sqrt{3}G-2}{\sqrt{3}G-1} \cdot \frac{\hat{i}_{\mathrm{ac}}}{\delta_C \cdot f_s \cdot V_{\mathrm{dc}}}$
MCPWM + 1P ST [17]	$L = \frac{1}{6\sqrt{3}} \cdot \frac{\sqrt{3}G-2}{\sqrt{3}G-1} \cdot \frac{V_{\mathrm{dc}}}{\delta_L \cdot f_s \cdot \hat{i}_{\mathrm{ac}}}$	$C = \frac{1}{8\sqrt{3}} \cdot \frac{\sqrt{3}G-2}{\sqrt{3}G-1} \cdot \frac{\hat{i}_{\mathrm{ac}}}{\delta_C \cdot f_s \cdot V_{\mathrm{dc}}}$
MPWM+1P/3P ST [16], IPWM+1P ST	$L = \frac{0.0181}{\sqrt{3}\pi} \cdot \frac{V_{\mathrm{dc}}}{\delta_L \cdot f_{\mathrm{Line}} \cdot \hat{i}_{\mathrm{ac}}}$	$C = \frac{0.0181G}{4(3\sqrt{3}G-\pi)} \frac{\hat{i}_{\mathrm{ac}}}{\delta_C \cdot f_{\mathrm{line}} \cdot V_{\mathrm{dc}}}$

Fig. 19.   Inductance requirement of Z-source inverter with different PWM strategies.

Appendix

$$I_{C\_\mathrm{rms}}^2 = \frac{6}{T_{\mathrm{Line}}} \sum \Delta(t) \cdot i_C^2(t)$$

$$= \frac{3}{\pi} \left[\int_0^{\pi/3} \left(d_{\mathrm{ST}}(\omega t) \cdot (i_C(\omega t))^2 \right. \right.$$

$$\left. \left. + d_{\mathrm{NST}}(\omega t) \cdot (i_C(\omega t))^2 \right) d(\omega t) \right]. \qquad (38)$$

Based on the equations listed in Table IV and the afore-mentioned definitions, the relationship of passive components requirements versus voltage gain for Z-source inverter with different PWM strategies is shown in Figs. 19 and 20. f_s/f_{line} is the ratio of switching frequency over the output voltage line frequency. The parameters K_L, K_C, and K_{C_rms} are defined as

$$K_L = \frac{L}{V_{\mathrm{dc}}/\delta_L f_s \hat{i}_{\mathrm{ac}}} \qquad (39)$$

$$K_C = \frac{C}{\hat{i}_{\mathrm{ac}}/\delta_C f_s V_{\mathrm{dc}}} \qquad (40)$$

$$K_{\mathrm{IC}} = \frac{I_{C\_\mathrm{rms}}}{\hat{i}_{\mathrm{ac}}} \qquad (41)$$

where K_L reflects the inductance requirement, and K_C and K_{IC} reflect the capacitance requirement and current ripples of capacitor.

Based on the equations listed in Table II, under the same input and output operation condition, Z-source inverter with different PWM strategies has the same average current i_L. With MPWM
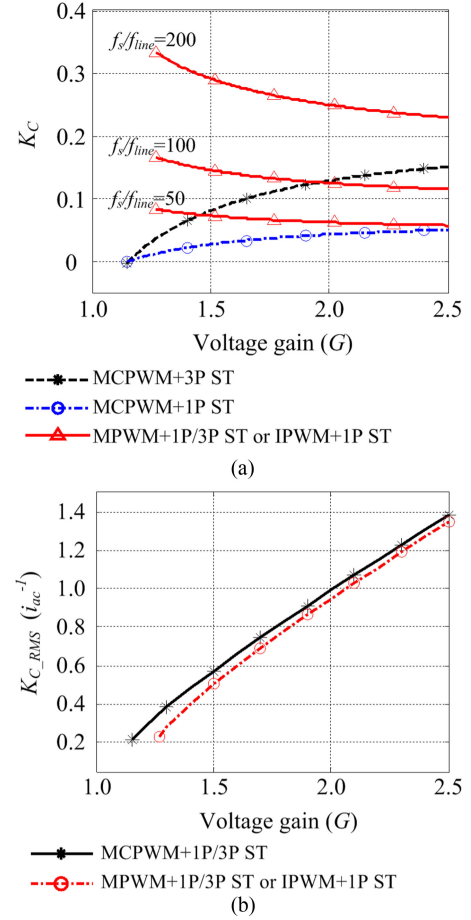
Fig. 20.   Capacitor requirement of Z-source inverter with different PWM strategies. (a) Capacitance comparison. (b) RMS current of capacitor.

strategies (MPWM + 1P/3P ST and IPWM + 1P ST), it has the minimum capacitor voltage v_C. As shown in Figs. 19 and 20, MCPWM + 1P ST has the least inductance and capacitance requirement. With the increase of switching frequency, MCPWM + 1P/3P ST needs much smaller inductance and capacitance compared to MPWM + 1P/3P ST and IPWM + 1P ST. However, much high switching frequency causes large switching losses of power devices. The tradeoff between the size of passive components and power devices loss should be considered in practical application. Compared to MCPWM + 1P/3P ST, MPWM + 1P/3P ST and IPWM + 1P ST reduce the rms value of capacitor current ripples.

V. CLOSED-LOOP CONTROLLER DESIGN

When Z-source inverter operates with constant boost control, there are two control variables: d_{ST} and M_i. The intermediate capacitor voltage v_C is controlled by d_{ST} and the output ac voltage is controlled by M_i, using separate controllers [27], [29]. However, when Z-source inverter operates with MPWM (IPWM + 1P ST), there is only one control freedom d_{ST} for both regulation of v_C and $\hat{v}_{\mathrm{ac}}$. Fig. 21 shows the closed-loop control system diagram, which consists of the dc-side dual-loop capacitor voltage control and the ac-side output voltage

Fig. 21. Control system diagram of Z-source inverter with IPWM + 1P ST.

control. For a given output voltage reference $\hat{v}_{\mathrm{ac}}^*$, voltage gain G and reference capacitor voltage v_C^* are calculated by (6) and (2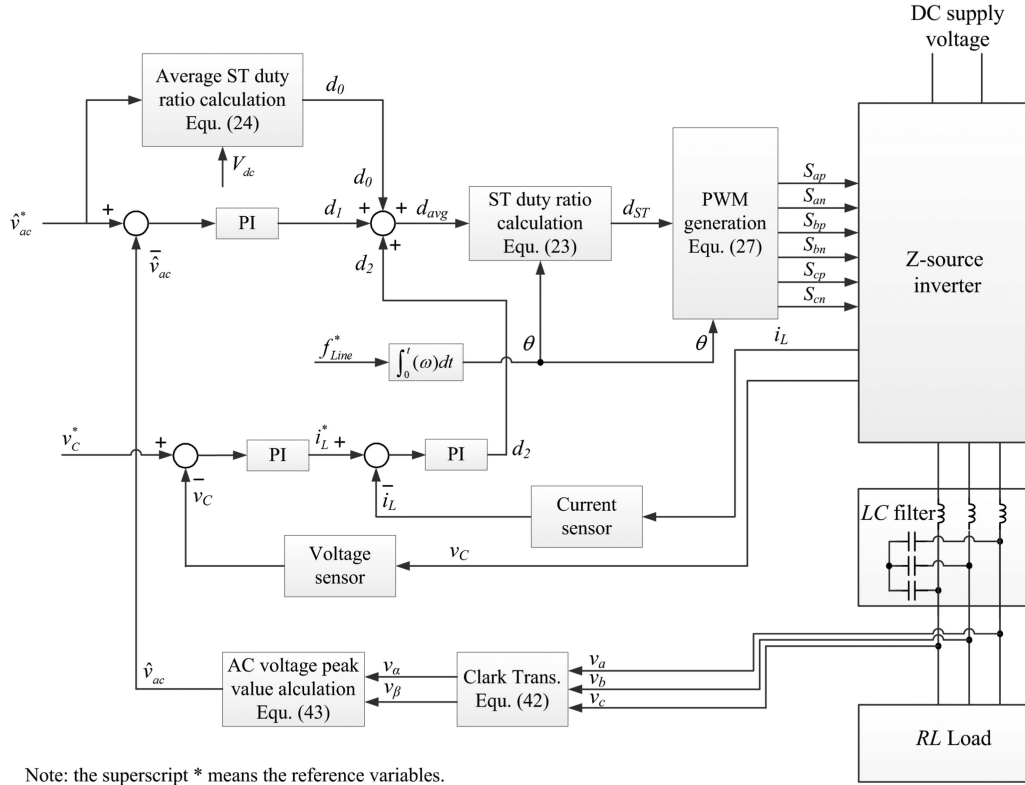2). With regarding to the nonlinear relationship of G and d_{avg} expressed in (24) and nonminimum phase characteristics of v_C and d_{avg} in (20), the feedforward control technique with $\hat{v}_{\mathrm{ac}}^*$ and input voltage V_{dc} is introduced to calculate the approximate value of average ST duty ratio d_0 by (24). This is beneficial to achieve a good transient performance. For ac-side control, the amplitude of three-phase voltage is feedback because it is dc component. v_{ao}, v_{bo}, and v_{co} are measured and transformed into v_α and v_β in two-axis stationary reference frame according to the following equation:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{42}$$

where factor 2/3 is included, which means that the amplitude of voltage vector equals to the peak value of the output phase voltage. Then, $\hat{v}_{\mathrm{ac}}$ can be calculated by

$$\hat{v}_{\mathrm{ac}} = \sqrt{v_\alpha^2 + v_\beta^2}. \tag{43}$$

The proportional-integral (PI) controller output d_1 makes sure three-phase output voltage follows the reference with zero steady-state error. The PI controller output d_2 drives the dc-side capacitor voltage to follow V_C^*. The phase angle θ determines which sextant the reference voltage vector is located in. The instantaneous ST duty ratio d_{ST} is calculated based on d_{avg} and θ according to (23). Then, the PWM module generates PWM
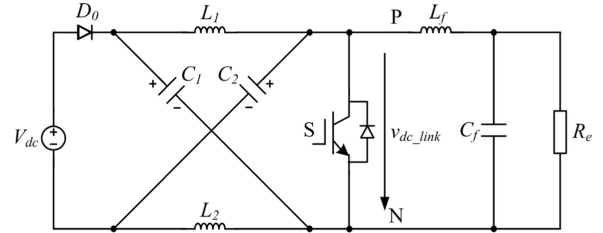
signals for six power devices in Z-source inverter according to (27).

The state-space averaged model provides good understanding of circuit characteristic and tools for parameters design of PI controller. For Z-source inverter supplying three-phase balanced load, the ac-side can be transferred to dc-side and simplified as a resistive load connected with an essential *LC* filter. Fig. 22 shows the dc-side equivalent circuit. The equivalent load resistor is calculated based on power balance

Fig. 22. DC-side equivalent circuit.

$$R_e = \frac{18}{\pi^2} \cdot R_L. \tag{44}$$

By taking all the inductor current (i_L, i_{Lf}) and capacitor voltage (v_C, v_{Cf}) as the state variables and using the state-space averaging method in one switching time period (T_s), the state equations of dc-side equivalent circuit can be expressed as

the following equation:

$$
\begin{bmatrix} \dfrac{di_L}{dt} \\ \dfrac{dv_C}{dt} \\ \dfrac{di_{Lf}}{dt} \\ \dfrac{dv_{Cf}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{1-2d_{\mathrm{ST}}}{L} & 0 & 0 \\ \dfrac{1-2d_{\mathrm{ST}}}{C} & 0 & -\dfrac{1-d_{\mathrm{ST}}}{C} & 0 \\ 0 & \dfrac{2(1-d_{\mathrm{ST}})}{L_f} & 0 & -\dfrac{1}{L_f} \\ 0 & 0 & \dfrac{1}{C_f} & -\dfrac{1}{C_f R_e} \end{bmatrix}
$$

$$
\times \begin{bmatrix} i_L \\ v_C \\ i_{Lf} \\ v_{Cf} \end{bmatrix} + \begin{bmatrix} \dfrac{1-d_{\mathrm{ST}}}{L} \\ 0 \\ -\dfrac{1-d_{\mathrm{ST}}}{L_f} \\ 0 \end{bmatrix} V_{\mathrm{dc}} \tag{45}
$$

$$
G_{i_L}(s) = \frac{\hat{i}_L(s)}{\hat{d}_{\mathrm{Son}}(s)}
$$
$$
= \frac{a_{13} \cdot s^3 + a_{12} \cdot s^2 + a_{11} \cdot s + a_{10}}{b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \tag{46}
$$

$$
G_{v_C}(s) = \frac{\hat{v}_C(s)}{\hat{d}_{\mathrm{Son}}(s)}
$$
$$
= \frac{a_{23} \cdot s^2 + a_{22} \cdot s^2 + a_{21} \cdot s + a_{20}}{b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \tag{47}
$$

$$
G_{v_{Cf}}(s) = \frac{\hat{v}_{Cf}(s)}{\hat{d}_{\mathrm{Son}}(s)}
$$
$$
= \frac{a_{32} \cdot s^2 + a_{31} \cdot s + a_{30}}{b_4 \cdot s^4 + b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s + b_0} \tag{48}
$$

where the numerator and denominator coefficients are as follows:

$$
a_{13} = CL_f C_f R_e \alpha,\ a_{12} = CL_f \alpha + (1-2D)C_f L_f R_e \beta
$$
$$
a_{11} = (1-2D)L_f \beta + CR_e \alpha + (1-\mathrm{D})C_f R_e \alpha,
$$
$$
a_{10} = 2(1-D)\alpha
$$
$$
a_{23} = -LL_f C_f R_e \beta
$$
$$
a_{22} = -LL_f \beta + [(1-D)L + (1-2D)L_f]C_f R_e \alpha,
$$
$$
a_{21} = [(1-D)L + (1-2D)L_f]\alpha - LR_e \beta,
$$
$$
a_{20} = (1-2D)R_e \alpha
$$
$$
a_{32} = -LCR_e \alpha,\ a_{31} = -2(1-D)LR_e \beta,
$$
$$
a_{30} = (1-2D)R_e \alpha
$$
$$
b_4 = LCL_f C_f R_e,\ b_3 = LCL_f
$$
$$
b_2 = LCR_e + (1-2D)^2 L_f C_f R_e + 2(1-D)^2 LC_f R_e
$$
$$
b_1 = 2(1-D)^2 L + (1-2D)^2 L_f,
$$

Fig. 23.   Block diagram of closed-loop controller for dc-side equivalent circuit.

$$
b_0 = (1-2D)^2 R_e
$$
$$
\alpha = 2V_C - V_{\mathrm{dc}} = \frac{1}{1-d_{\mathrm{ST}}}V_{\mathrm{dc}},
$$
$$
\beta = 2I_L - I_{Lf} = \frac{1}{(1-d_{\mathrm{ST}})^2}\frac{V_{\mathrm{dc}}}{R_e}.
$$

Performing small signal perturbation at the equilibrium operation point, the transfer functions of control to inductor current, intermediate capacitor voltage, and output voltage perturbations are derived as (46), (47), and (48), respectively.

It can be observed from (46) to (48) that the transfer functions of ST duty ratio to intermediate capacitor voltage $G_{v_C}(s)$ and output voltage $G_{v_{Cf}}(s)$ contains the right-half-plane (RHP) zeroes. With RHP zeroes, the expected voltage falls before rising to the reference when the step increase of control command is given [27]. This nonminimum phase system exhibits a worse dynamic response and causes oscillation. Usually, the inner current loop is essential to deal with such an influence and to obtain the good response.

Fig. 23 shows the block diagram of dc-side closed-loop controller. $C_i(z)$ $C_{v_C}(z)$, and $C_{v_{Cf}}(z)$ are the typical digital PI controller with antiwindup correction expressed in (49). H_i and H_{vc}, H_{vcf} are the coefficients of current and voltage sampling units, respectively. $(1 - e^{-T_s s})/s$ is zero-order hold. $e^{-T_d s}$ is time delay. $G_{i_L}(s)$, $G_{v_C}(s)$, and $G_{v_{Cf}}(s)$ are the control to state variable transfer functions expressed in (46)–(48). $G_{i_L}(s)$ is the minimum phase system transfer function. And the total phase delay is 90°. Therefore, the inner current regulator $C_i(z)$ is easily designed to meet the bandwidth requirement. $C_{v_{Cf}}(z)$ provides the guidance for controller parameters design for ac output voltage. Applying the formula for Mason's rule, the inner current closed-loop transfer function is derived as (50). Once the current loop is designed, it can be treated as a new power stage for the outer voltage loop design. The closed-loop transfer functions of capacitor voltage and filtered output voltage are derived as (51) and (52)

$$
G_c(z) = K_p + K_i T_s \cdot \frac{z}{z-1} \tag{49}
$$

$$
T_{i_L}(s) = \frac{C_i(s) \cdot G_{i_L}(s)}{1 + H_i \cdot C_i(s) \cdot G_{i_L}(s)} \tag{50}
$$

$$
T_{v_C}(s) = \frac{C_{v_C}(s) \cdot T_{i_L}(s) \cdot G_{v_C}(s)}{G_{i_L}(s) + H_{v_C} \cdot C_{v_C}(s) \cdot T_{i_L}(s) \cdot G_{v_C}(s)} \tag{51}
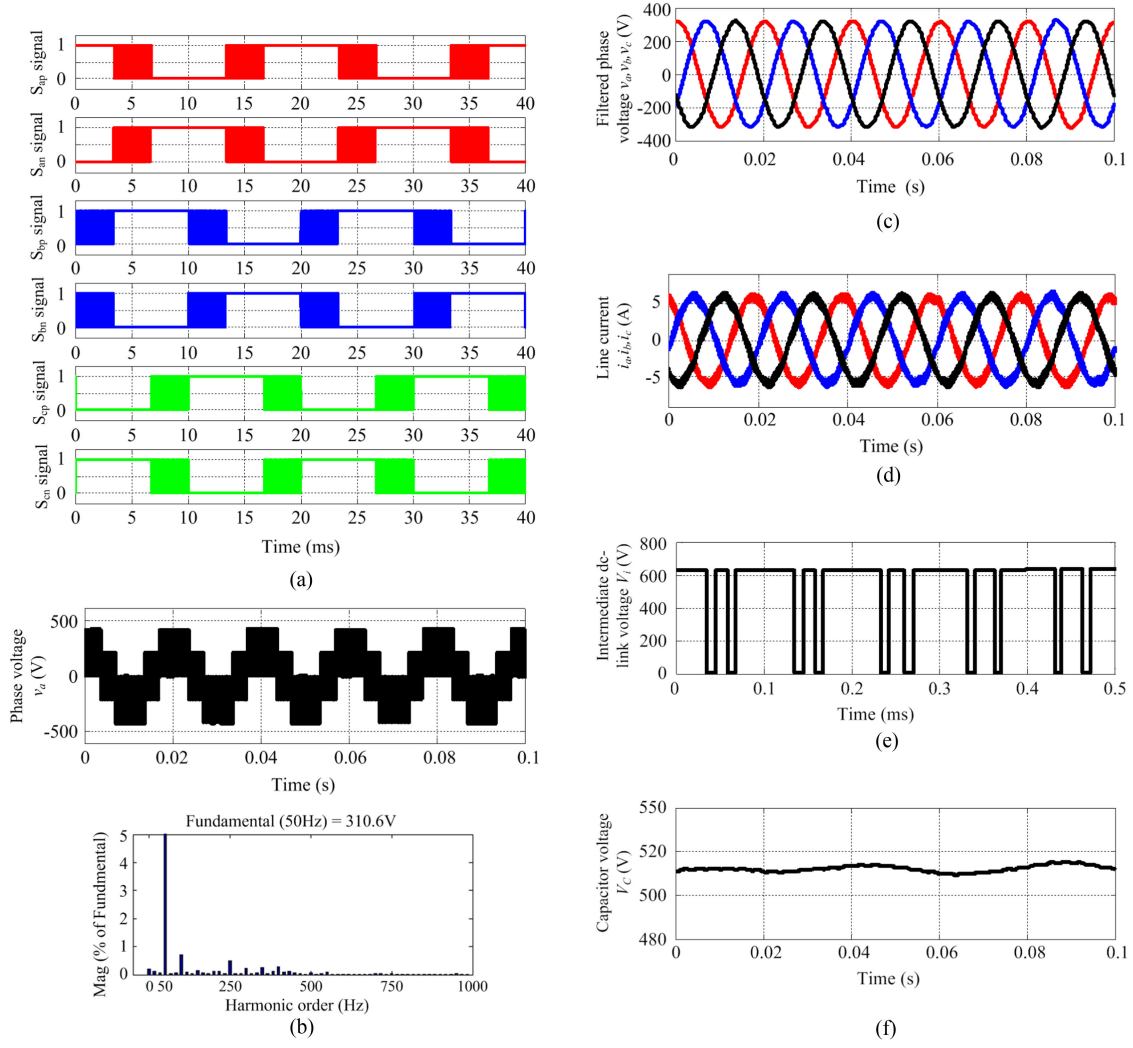$$

Fig. 24. Simulation results for Z-source inverter with IPWM + 1P ST. (a) Drive signal. (b) Output phase voltage and spectrum analysis. (c) Filtered output phase voltage. (d) Output line current. (e) Intermediate dc-link voltage. (f) Capacitor voltage.

$$T_{v_{C_f}}(s) = \frac{C_{v_{C_f}}(s) \cdot T_{i_L}(s) \cdot G_{v_{C_f}}(s)}{C_{i_L}(s) \cdot G_{i_L}(s) + H_{v_{C_f}} \cdot C_{v_{C_f}}(s) \cdot T_{i_L}(s) \cdot G_{v_{C_f}}(s)}.$$

$$(52)$$

VI. SIMULATION AND EXPERIMENT VERIFICATION

Numerical simulations using MATLAB/Simulink have been performed to verify IPWM + 1P ST and theoretical analysis. The main circuit parameters are: $V_{dc} = 300-400$ V, $L = 8$ mH, $C_1 = C_2 = 330$ μF, $L_f = 400$ μH, $C_f = 25$ μF, $R_{Load} = 60$ Ω, $L_{load} = 2$ mH. The switching time period T_s is 100 μs. The output line frequency is $f_{line} = 50$ Hz. The current/voltage ripple coefficients of inductor/capacitor for Z-source network are preset as $\delta_L = 0.4$, $\delta_C = 0.0015$ under the maximum operation condition $G = 2.1$, $i_L = 10$ A, and $V_C = 600$ V. The cutoff frequency of low-pass filter in output side is set about 2 kHz ($f_c = 1/5f_s$) to attenuate the switching frequency ripples.

Fig. 24 shows the captured waveforms of Z-source inverter with IPWM + 1P ST under the output reference voltage of $\hat{v}_{ac} = 310$ V. According to (6) and (22), the voltage gain $G = 1.56$, and the capacitor voltage $V_C = 514.6$ calculated in theory are identical to the simulation results. Compared with the existing PWM strategies, Z-source inverter with IPWM + 1P ST achieves the maximum voltage gain as well as minimum voltage stress and switching frequency of power devices.

A laboratory prototype rated at 2.5 kW was built to confirm the IPWM strategy with Infineon power devices. Fig. 25 shows a photograph of the test platform. The main control board is designed based on DSP28335. The drive circuit of IGBT is designed with ACPL-330J based on the existing mature technology. A programmable dc power supply is arranged as the dc source to simulate the $V - I$ characteristics of fuel cells and solar arrays. A Y-type three-phase RL load is connected to the ac side of the inverter. HIOKI 3390 power analyzer simultaneously measures the input dc power and ac output power to perform efficiency analysis. The time duration of each switching instant is precalculated in DSP28335. The conditioning board performs logic operations to generate gate signals of power devices according to the requirement of
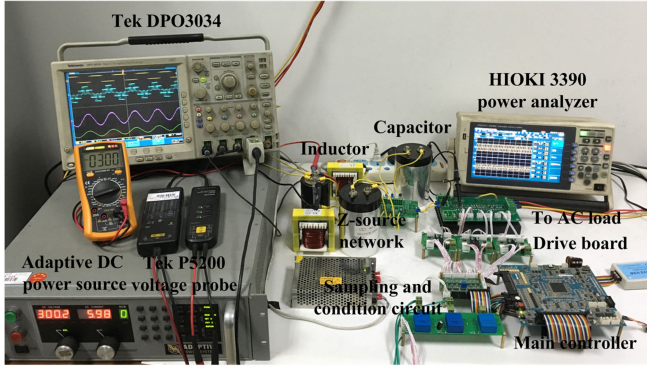
Fig. 25.   Z-source inverter test platform.

TABLE V
SPECIFICATIONS FOR THE EXPERIMENTAL PROTOTYPE

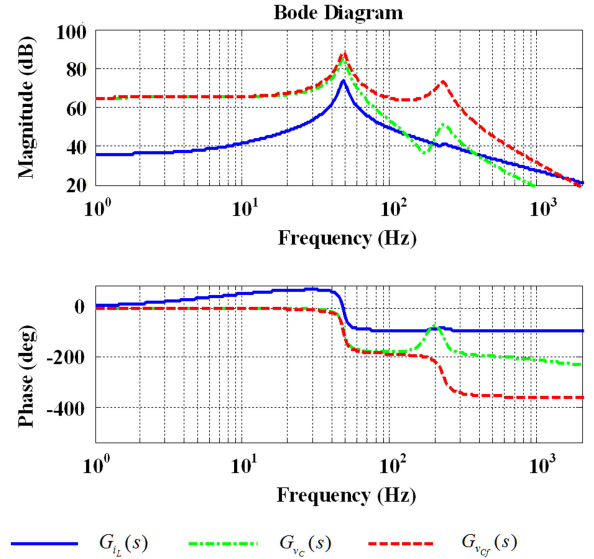| Switching device	Front-end diode S_{ap}, S_{an}, S_{bp}, S_{bn}, S_{cp}, S_{cn}	DIODE (IDP30E120) IGBT(IGW25N120) and DIODE(IDP18E120)
Passive components	L	8 mH
	C_1 and C_2	330 μF
Three-phase EMI filer	L_f	400 μH
	C_f	35 μF
Three-phase RL load	R_{load}	$40 - 300\ \Omega$
	L_{load}	2 mH
Switching time period	T_s	100 μs
Current sensor	H_i	0.1
Voltage sensor	H_{vc} and H_{vcf}	0.01

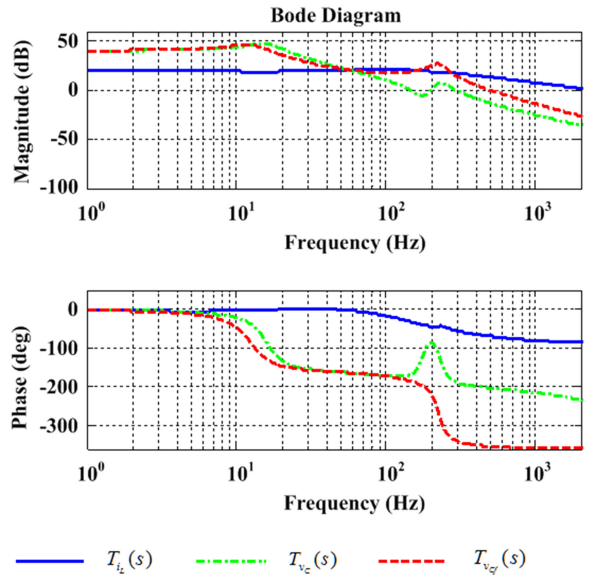Fig. 26.   Frequency characteristic of control to inductor current, intermediate capacitor voltage, and output voltage.

Fig. 27.   Closed-loop frequency response of inductor current, intermediate capacitor voltage, and output voltage.

the output voltage vector. The specifications for the experimental prototype are listed in Table V. The key parameters of closed-loop controllers are $G_{i_L}(z) = 0.11 + 0.0035 \cdot z/(z - 1)$; $G_{vC}(z) = 0.06 + 0.012 \cdot z/(z - 1)$; $G_{vCf}(z) = 0.048 + 0.03 \cdot z/(z - 1)$.

For Z-source inverter with IPWM + 1P ST, the inductor current in the impedance network inevitably contains 300 Hz low-frequency ripples for 50 Hz ac output. Fig. 26 shows the frequency characteristic of control to inductor current, intermediate capacitor voltage, and filtered output voltage. In order to suppress the undesired influence of low frequency ac components, the bandwidth of inner current loop is designed below 300 Hz. Fig. 27 shows the designed closed-loop frequency responses. The inner current loop is designed with 200 Hz bandwidth and 45° phase margin. The intermediate capacitor voltage loop and output voltage loop are designed with almost 25 Hz bandwidth and 30° phase margin, which is beneficial to reduce the voltage oscillatory.

Fig. 28 shows the experiment results for Z-source inverter with IPWM + 1P ST under the output reference voltage of $\hat{v}_{ac} = 310$ V when the input voltage $V_{dc} = 300 - 400$ V. The maximum voltage gain of $G = 2.07$ can be obtained. Fig. 28(a) shows the voltage waveforms of gate signals for power devices (S_{ap}, S_{bp}, and S_{cp}). During each sextant, the switches in the legs of v_{max} and v_{min} are fixed. Only switches in one phase leg of v_{mid} are commutating with PWM. Fig. 28(b) shows the captured waveforms of the intermediate dc-link voltage, the output phase

voltage before and after the filter, as well as the output current. By adjusting the ST to maintain the filtered output phase voltage is 220 V/50 Hz, the measured intermediate capacitor voltage is about 517.8 V, which is a little larger than the theoretical values of 514 V. This is due to the voltage drop and power loss of switches in the inverter bridge. Compared with existing PWM strategies, IPWM + 1P ST achieves the minimum intermediate dc-link capacitor voltage and equivalent switching frequency.
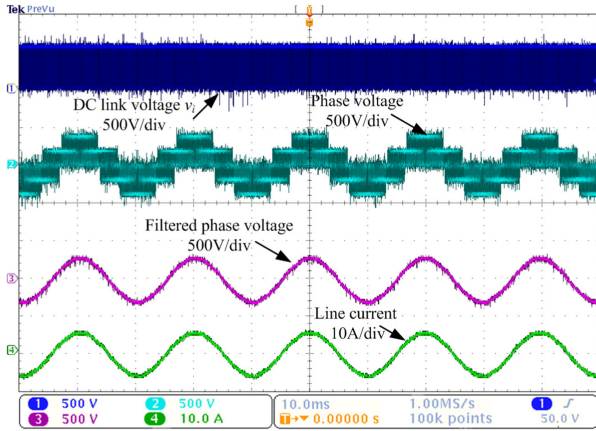
The maximum boost PWM strategy introduces six-time-line-frequency ripples in the dc-side inductor current and the capacitor voltage. Therefore, it is more suitable for 400–800 Hz medium frequency application of power supply system due to a relatively high output line frequency. Fig. 29 shows the captured waveforms for Z-source inverter using IPWM + 1P ST when the
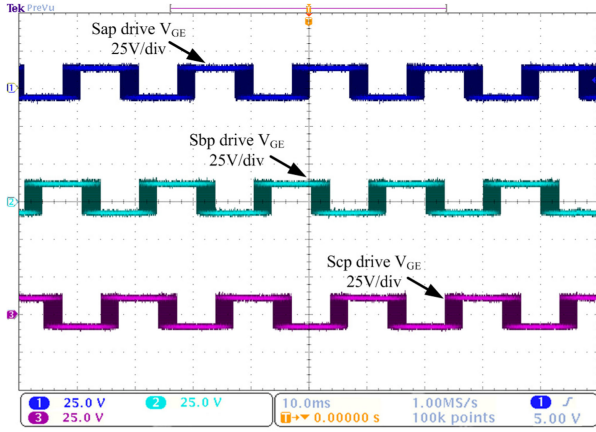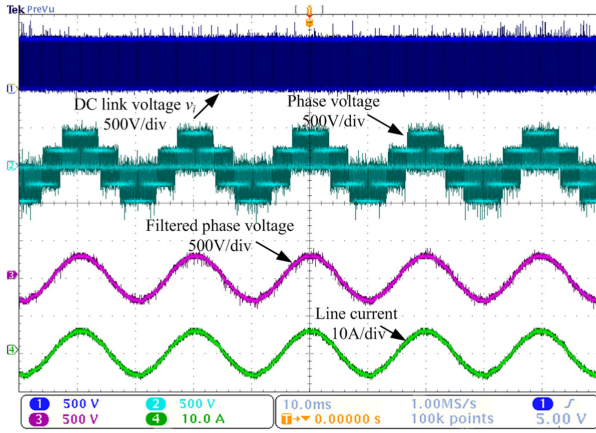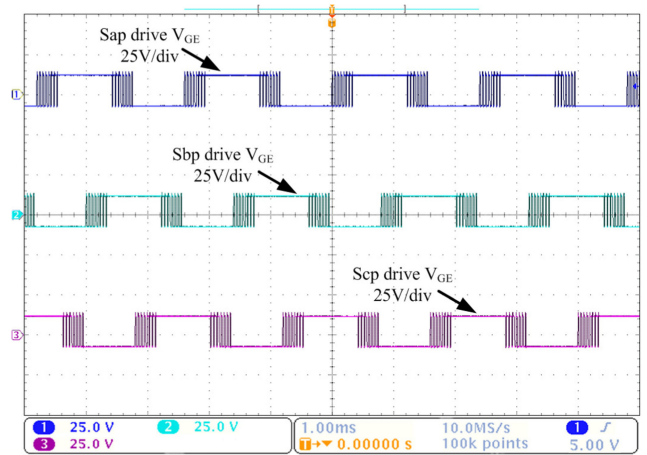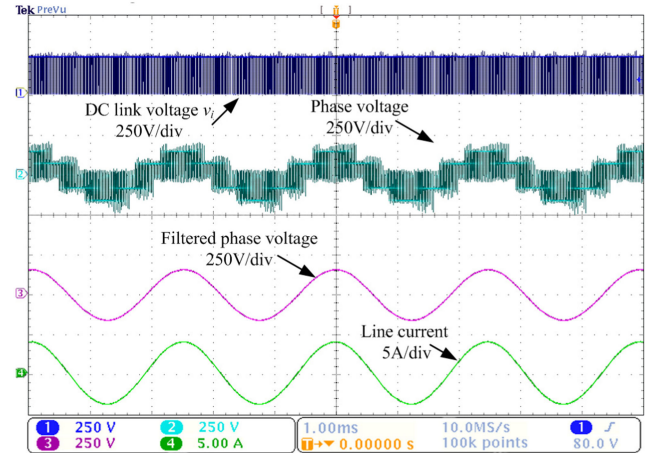
Fig. 28. Z-source inverter with IPWM+1P ST ($R_L = 60\ \Omega$, $f_{\text{line}} = 50\ \text{Hz}$). (a) Power device gate signals. (b) Intermediate dc-link voltage, output voltage, and current ($V_{\text{dc}} = 300\ \text{V}$). (c) Intermediate dc-link voltage, output voltage, and current ($V_{\text{dc}} = 400\ \text{V}$).

Fig. 29. Z-source inverter with IPWM + 1P ST ($V_{\text{dc}} = 200\ \text{V}, R_L = 40\ \Omega$, $f_{\text{line}} = 400\ \text{Hz}$). (a) Voltage waveforms of power device gate signals. (b) Intermediate dc-link voltage, output voltage, and current ($V_{\text{dc}} = 200\ \text{V}$).

output phase voltage is 110 V/400 Hz, the dc source voltage is $V_{\text{dc}} = 200$ V, and the switching time period is $T_s = 50\ \mu$s. The maximum voltage gain of $G = 1.56$ can be obtained. The measured intermediate capacitor voltage 261.3 V is quite consistent with the theoretical value 258 V calculated from (22).

Fig. 30(a) and (b) shows the experimental results when the reference output voltage $\hat{v}_{\text{ac}}^*$ has a step change from 250 V to 310 V

and back to 250 V, respectively. The controller is stable under steady state operation and the step change response is also fast with acceptable response time. With controller design shown in Fig. 21, the output three-phase voltage has good transient performance. The output three-phase voltage follows the reference when the intermediate capacitor voltage $V_C = 413.5$ V achieves new steady state $V_C = 514.4$ V. Fig. 31(a) and (b) shows the experimental results when the load resistance has a step change from $R_L = 160\ \Omega$ to $R_L = 120\ \Omega$ and back to $R_L = 160\ \Omega$, respectively. The dc-side capacitor voltage and output ac voltage recover quickly.

The losses of power converter include semiconductor devices losses, passive components losses, controller and driver losses, etc. Among them, the semiconductor devices losses are the dominant part. IGBT losses consist of turn-on and turn-off switching losses besides conduction losses. DIODE losses include the reverse recovery losses and conduction losses because the turn-on losses are small enough to be neglected [35]. The switching losses model of semiconductor device can be expressed as
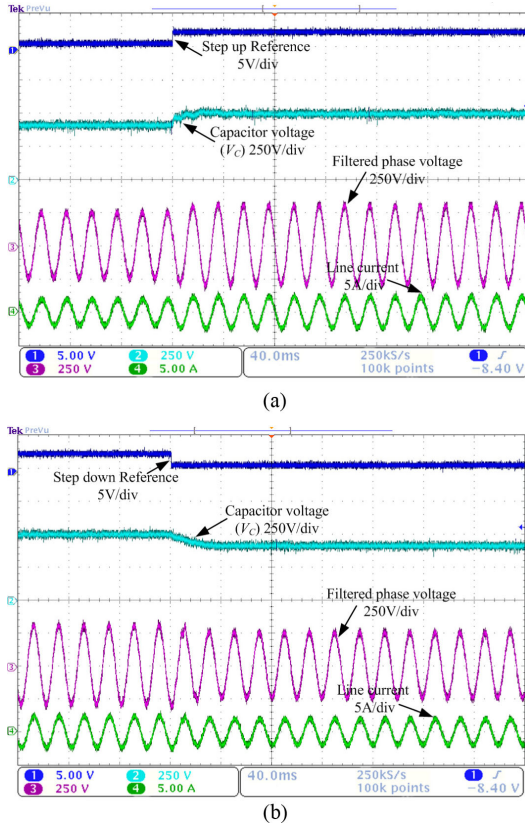
(a)

(b)

Fig. 30.   Dynamic responses of Z-source inverter under step change of output voltage reference ($V_{dc} = 300$ V, $R_L = 120$ Ω). (a) Step up 250–310 V. (b) Step down 310–250 V.

(a)

(b)

Fig. 31.   Dynamic responses of Z-source inverter under step change of load resistance ($V_{dc} = 300$ V, $\hat{v}_{ac} = 350$ V). (a) Step change of R_L from 160 Ω to 120 Ω. (b) Step change of R_L from 120 Ω to 160 Ω.

follows [35]–[37]:

$$E_{sw(on,off)} = (\alpha + \beta \cdot i_{sw} + \gamma \cdot i_{sw}^2)\frac{V_{sw}}{V_{ref}} \qquad (53)$$

$$P_{sw} = f_{sw} \cdot (E_{swon} + E_{swoff}) \qquad (54)$$

where V_{sw} is the blocking voltage, i_{sw} is the switched current, α, β, γ are the device parameters from the datasheet, and V_{ref} is the reference voltage under which device parameters are derived.

The conduction losses of the front-end diode and switches in the inverter bridge can be calculated by

$$P_{con\_dc} = \frac{1}{T_s}\int_{t_1}^{t_2} v_{con} \cdot i_{con} dt \qquad (55)$$

$$P_{con\_inv} = \frac{1}{2\pi}\int_{\lambda_1}^{\lambda_2} d_{con} \cdot v_{on} \cdot i_{con} d\theta_r \qquad (56)$$

where $v_{con} = v_{th} + ri_{con}$ is the on-state voltage drop, v_{th} is the threshold voltage, r is the on-state resistor, i_{con} is the conduction current, and d_{con} is the conduction duration.

According to the power devices losses model, the switching losses and conduction losses of each power device can be calculated for theoretical analysis. Fig. 32 shows the losses distribution of Z-source inverter with different PWM strategies operating at normal condition as a reference. IGBT switching losses and front-end DIODE D_0 reverse recovery losses occupy the main part. Therefore, the reduction of switching frequency
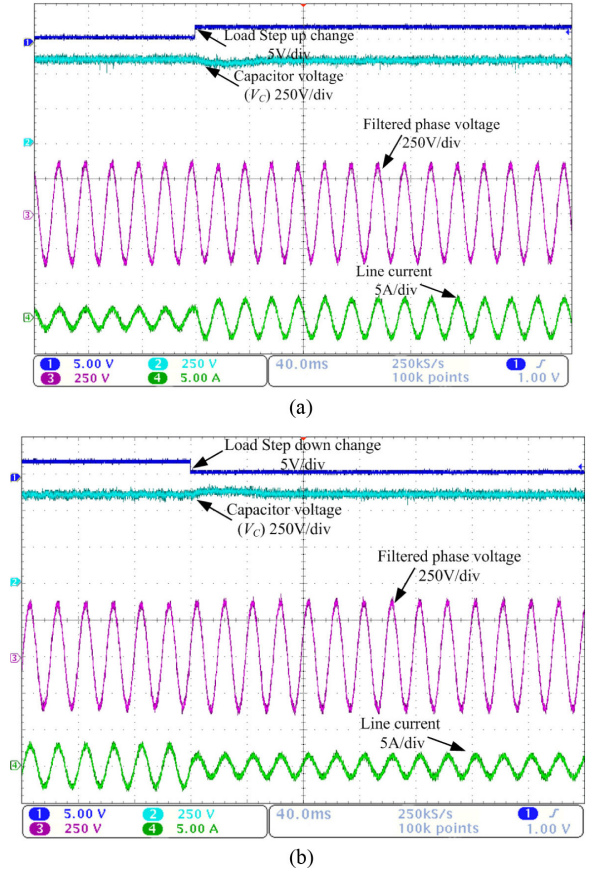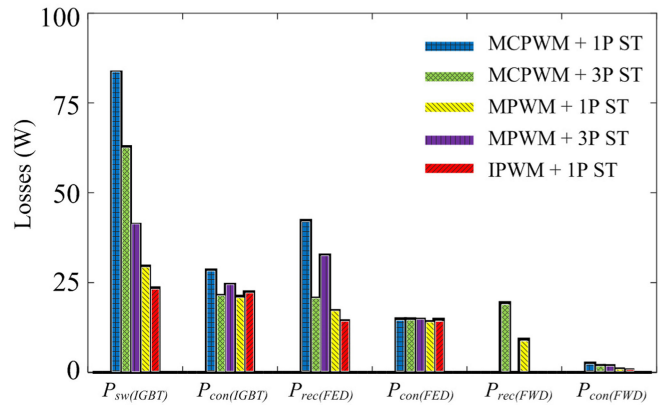

Fig. 32.   Theoretical analysis of losses distribution for Z-source inverter with different PWM strategies ($V_{dc} = 300$ V, $\hat{v}_{ac} = 311$ V, $P_o = 2500$ W, $T_s = 100$ μs).

and voltage stress is of great importance for efficiency improvement. The conduction loss of free-wheeling diode is the minor part. All the PWM strategies only have a slight difference in the conduction losses of IGBT and D_0. This is because by using different PWM strategies, IGBT and D_0 have almost the same average current stress in Figs. 15(b) and 17(b), respectively. MCPWM + 1P ST has the maximum IGBT switching losses due to a larger ST current compared with 3P ST method.
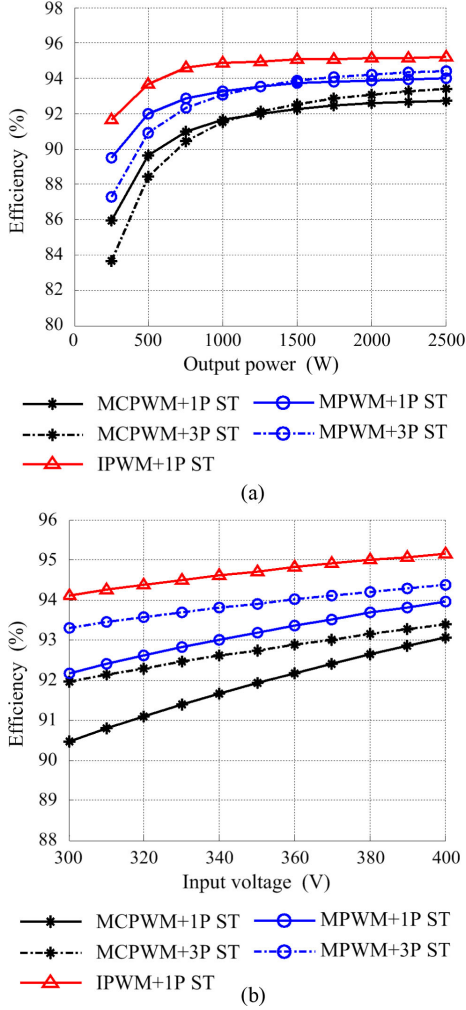
Fig. 33. Efficiency comparison of Z-source inverter with different PWM strategies. (a) Efficiency versus output power ($V_{dc} = 400$ V, $\hat{v}_{ac} = 311$ V, $P_o = 250$–2500 W). (b) Efficiency versus input voltage ($V_{dc} = 300$–400 V, $\hat{v}_{ac} = 311$ V, $P_o = 2500$ W).

Fortunately, for MCPWM + 1P ST in Fig. 5, MPWM + 1P ST in Fig. 7, and IPWM + 1P ST in Fig. 11, the ST interval is inserted at the instants of switching commutation between antiparalleled diode and IGBT. All the free-wheeling diodes in the inverter bridge achieve zero current turn OFF. Thus, free-wheeling diodes have almost no reverse recovery losses [34]. The turn-on losses of IGBT can be reduced too. Because the reduced switching frequency of IGBT and the front-end diode contributes to lowering power device losses, IPWM + 1P ST achieves the highest efficiency.

In order to quantify the improvement introduced by IPWM + 1P ST, the main circuit efficiency of Z-source inverter with different PWM strategies is measured under different output power and input voltage. Fig. 33 shows the efficiency comparison results of Z-source inverter operating at (a) $V_{dc} = 400$ V, $\hat{v}_{ac} = 311$ V, $P_o = 250 - 2500$ W by the change of load resistance, and (b) $V_{dc} = 300 - 400$ V, $\hat{v}_{ac} = 311$ V, $P_o = 2500$ W by the change of input voltage. The efficiency is increased with the decrease of voltage gain. Compared with existing PWM
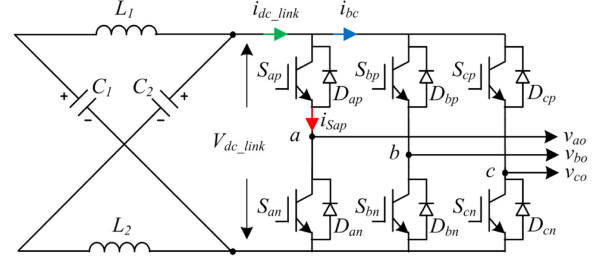

Fig. 34. Current of S_{ap} during ST state for PWM strategies with 1P ST.

strategies, Z-source inverter with IPWM + 1P ST demonstrates best efficiency due to the reduced switching frequency and voltage stress of power devices.

VII. CONCLUSION

This paper presents an IPWM strategy for Z-source inverter, which can minimize the voltage stress and switching frequency of power devices. Simulation and experiment results validate the theoretical analysis. Compared with existing PWM strategies, Z-source inverter with the IPWM demonstrates higher efficiency under full operation range of low voltage gain $(1.27 - 2)$ application. However, the dc-side inductor current and capacitor voltage contain six-time-line-frequency ripples, which consequently require large size of the passive components when the output frequency is very low. Thus, it is also suitable for 400–800 Hz medium frequency aircraft and vessel power supply system due to a relatively high output line frequency. Furthermore, the idea of IPWM strategy can be extended to other kinds of three-phase impedance network-based inverters.

APPENDIX

1) Current Stress Derivation of IGBT and Free-Wheeling Diode

Because of the symmetry, each IGBT and free-wheeling diode in the inverter bridge has the same current stress. Thus, only IGBT S_{ap} and diode D_{an} are analyzed, for example.

(1) MCPWM + 1P ST

During ST interval, D_0 is blocked. As shown in Fig. 34, i_{Sap} is i_{dc_link} minus i_{bc}. i_{dc_link} is $2i_L$. i_{bc} represents the sum of current across S_{bp} and S_{cp}, which depends on the current and switching states of phase b and c

$$i_{Sap} = i_{dc\_link}(\omega t) - i_{bc}(\omega t) = 2i_L - i_{bc}(\omega t) \quad (57)$$

$$i_{bc} = S_{bp} \cdot i_b(\omega t) + S_{cp} \cdot i_c(\omega t). \quad (58)$$

According to (57) and (58), ST current across S_{ap} in different sextants can be derived as

$$i_{S1(ig)\_ST}(\omega t) = \begin{cases} 2i_L & \left(-\dfrac{\pi}{3} \le \omega t \le \dfrac{\pi}{3}\right) \\ 2i_L - i_b(\omega t) & \left(\dfrac{\pi}{3} \le \omega t \le \dfrac{\pi}{2}\right) \\ 2i_L - i_c(\omega t) & \left(-\dfrac{\pi}{2} \le \omega t \le -\dfrac{\pi}{3}\right) \end{cases}.$$

$$(59)$$

From (59), the maximum instant current through S_{ap} occurs during ST interval $i_{p\_\mathrm{IGBT}} = 2i_L$. The ST interval d_{ST} is obtained from Table II.

During non-ST interval, S_{ap} and D_{an} conduct when i_a is positive $(-\pi/2 \leq \omega t \leq \pi/2)$. The conduction current is i_a. Thus, the maximum instant current through D_{an} is peak value of load current $i_{p\_\mathrm{FW\_DIODE}} = \hat{i}_{\mathrm{ac}}$. As shown in Fig. 5, the on-state interval of S_{ap} and D_{an} in a half line cycle can be derived as the following equations:

$$d_{\mathrm{Sap(IGBT)\_NST}}(\omega t)$$

$$= \begin{cases} V_{\mathrm{Sap(San)}}(\omega t) - \dfrac{d_{ST}(\omega t)}{6} & \left(\dfrac{\pi}{3} \leq \omega t \leq \dfrac{\pi}{2}\right) \\[2mm] V_{\mathrm{Sap(San)}}(\omega t) + \dfrac{d_{ST}(\omega t)}{6} & \left(-\dfrac{\pi}{3} \leq \omega t \leq \dfrac{\pi}{3}\right) \\[2mm] V_{\mathrm{Sap(San)}}(\omega t) - \dfrac{d_{ST}(\omega t)}{6} & \left(-\dfrac{\pi}{2} \leq \omega t \leq -\dfrac{\pi}{3}\right) \end{cases} \quad (60)$$

$$d_{\mathrm{San(Diode)\_NST}}(\omega t)$$

$$= \begin{cases} 1 - d_{\mathrm{Sap(IGBT)\_NST}}(\omega t) - \dfrac{d_{\mathrm{ST}}(\omega t)}{2} & \left(-\dfrac{\pi}{3} \leq \omega t \leq \dfrac{\pi}{3}\right) \\[2mm] 1 - d_{\mathrm{Sap(IGBT)\_NST}}(\omega t) - \dfrac{d_{\mathrm{ST}}(\omega t)}{6} & \left(\dfrac{\pi}{3} \leq \omega t \leq \dfrac{\pi}{2}\right) \\[2mm] 1 - d_{\mathrm{Sap(IGBT)\_NST}}(\omega t) - \dfrac{d_{\mathrm{ST}}(\omega t)}{6} & \left(-\dfrac{\pi}{2} \leq \omega t \leq -\dfrac{\pi}{3}\right) \end{cases}$$
$$(61)$$

2) MPWM + 1P ST

For MPWM + 1P ST, the main difference from MCPWM + 1P is the periodically varied d_{ST} in (10). D_{an} is always turned OFF in the first sextant. Thus, the maximum instant current occurs at the beginning of the second sextant. It is half of load peak current $i_{p\_\mathrm{FW\_diode}} = 0.5\hat{i}_{\mathrm{ac}}$. Substituting (10) into (60) and (61), the key parameters for current stress analysis can be obtained.

3) IPWM + 1P ST

For IPWM + 1P ST, ST interval is inserted in phase a in the second sextant $(\pi/3 \leq \omega t \leq 2\pi/3)$. Thus, the maximum instant currents of IGBT and free-wheeling diode occur at the beginning of the second sextant. $i_{p\_\mathrm{IGBT}} = 2i_L - 0.5\hat{i}_{\mathrm{ac}}$. $i_{p\_\mathrm{FW\_diode}} = 0.5\hat{i}_{\mathrm{ac}}$.

4) MCPWM + 3P ST

For MCPWM + 3P ST, during ST interval, all the switches in the inverter bridge are turned ON. Assuming the on-state resistors of each switch have the same value shown in Fig. 35, the current across S_{ap} and S_{an} meet

$$\begin{cases} i_{\mathrm{Sap}}(\omega t) + i_{\mathrm{San}}(\omega t) = \dfrac{4}{3} i_L \\[2mm] i_{\mathrm{Sap}}(\omega t) - i_{\mathrm{San}}(\omega t) = i_a(\omega t) \end{cases}. \quad (62)$$

From (62), the ST current through S_{ap} can be derived as

$$i_{\mathrm{Sap}}(\omega t) = \frac{2}{3} i_L + \frac{1}{2} i_a(\omega t). \quad (63)$$
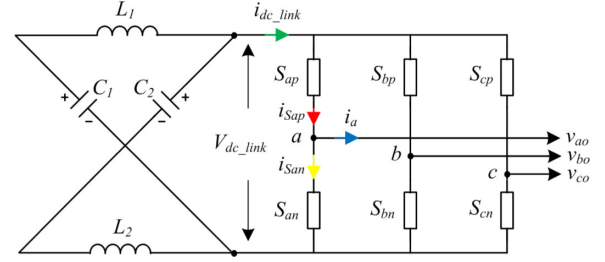

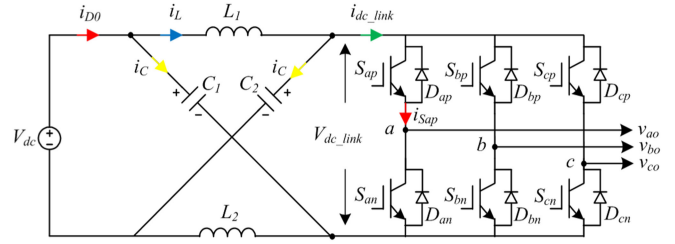Fig. 35. Current of S_{ap} during ST interval for MCPWM + 3P ST and MPWM+3P ST.

Fig. 36. Current analysis of D_0 during non-ST interval.

From (63), the maximum instant current through IGBT during ST interval is

$$i_{p\_\mathrm{IGBT}} = \frac{2}{3} i_L + \frac{1}{2} \hat{i}_{\mathrm{ac}}. \quad (64)$$

Seen from Fig. 35, during non-ST interval, the conduction current across S_{ap} and D_{an} is phase current i_a, but the conduction duration of S_{ap} and D_{an} decreases by $d_{\mathrm{ST}}/2$ compared with conventional three-phase VSI

$$d_{\mathrm{Sap\_NST}}(\omega t) = V^*_{\mathrm{Sap(San)}}(\omega t) - \frac{1}{2} d_{\mathrm{ST}}(\omega t) \quad (65)$$

$$d_{\mathrm{Dan\_NST}}(\omega t) = 1 - V^*_{\mathrm{Sap(San)}}(\omega t) - \frac{1}{2} d_{\mathrm{ST}}(\omega t). \quad (66)$$

(5) MPWM + 3P ST

For MPWM + 3P ST, the key parameters of current stress analysis can be obtained by substituting (10) into (65) and (66). D_{an} is always turned OFF in the first sextant. Thus, the maximum instant current occurs at the beginning of the second sextant $i_{p\_\mathrm{FW\_diode}} = 0.5\hat{i}_{\mathrm{ac}}$.

2) Current Stress Derivation of the Front-End Diode

As for Z-source inverter, D_0 is conducting during non-ST interval and the equivalent circuit is shown in Fig. 36. i_{D0} can be expressed as $2i_L - i_{\mathrm{dc\_link}}$. In one switching time period, $i_{\mathrm{dc\_link}}$ changes among zero and different load current

$$i_{D0\_\mathrm{NST}}(\omega t) = i_L(\omega t) + i_C(\omega t) = 2i_L(\omega t) - i_{\mathrm{dc\_link}}(\omega t)$$
$$(67)$$

$$i_{\mathrm{dc\_link}}(\omega t) = S_{\mathrm{ap}}(\omega t)i_a(\omega t) + S_{\mathrm{bp}}(\omega t)i_b(\omega t)$$
$$+ S_{\mathrm{cp}}(\omega t)i_c(\omega t). \quad (68)$$

In the first sextant, i_{D0} in different switching state is

$$i_{\text{FE(Diode)}}(\omega t) = \begin{cases} 2i_L & (111\,000) \\ 2i_L - i_a(\omega t) & (100) \\ 2i_L + i_c(\omega t) & (110) \end{cases}. \quad (69)$$

The corresponding duty ratio of different switching state is

$$\begin{cases} d_{(111,000)}(\omega t) = 1 - V^*_{\text{Sap(San)}}(\omega t) & (111\,000) \\ \quad + V^*_{\text{Scp(Scn)}}(\omega t) - d_{\text{ST}}(\omega t) \\ d_{(100)}(\omega t) = V^*_{\text{Sap(San)}}(\omega t) - V^*_{\text{Sbp(Scn)}}(\omega t) & (100) \\ d_{(110)}(\omega t) = V^*_{\text{Sbp(Scn)}}(\omega t) - V^*_{\text{Scp(Scn)}}(\omega t) & (110) \end{cases} \quad (70)$$

With MCPWM + 1P ST and MCPWM + 3P ST, the peak current of D_0 occurs in zero switching state, which is $2i_L$. With MPWM + 1P ST and MPWM + 3P ST, there is no zero switching state in non-ST interval. From (69), the peak current of D_0 is

$$i_{P\_\text{FE(Diode)}} = 2i_L - \frac{1}{2}i_{ac} = \left(\frac{3}{2} \cdot G - \frac{1}{2}\right)i_{ac}. \quad (71)$$

With different PWM strategies, the interval of active voltage vectors can be obtained from (70).

3) Passive Components Ripples Derivation
(1) MCPWM + 1P ST and MCPWM + 3P ST

A. Inductor Requirement

As shown in Fig. 10, during ST interval, $V_L = V_C$ and i_L is increasing. And during non-ST interval, $V_L = V_{\text{dc}} - V_C$ and I_L is decreasing. The average voltage across inductor in one switching time period is zero.

For MCPWM + 1P ST in Fig. 4 and MCPWM + 3P ST in Fig. 5, each ST interval is $1/2d_{\text{st}}T_s$ and $1/6d_{\text{st}}T_s$, respectively. Thus, the inductor current ripples can be appropriately calculated based on d_{ST} and V_C

$$\Delta i_L = \frac{1}{L} \cdot V_C \cdot \frac{d_{ST}}{2}T_s \quad \text{For MCPWM + 3P ST} \quad (72)$$

$$\Delta i_L = \frac{1}{L} \cdot V_C \cdot \frac{d_{ST}}{6}T_s \quad \text{For MCPWM + 1P ST.} \quad (73)$$

Substituting V_C and d_{ST} listed in Table II into (72) and (73), Δi_L can be rewritten as

$$\Delta i_L = \frac{\sqrt{3} \cdot (\sqrt{3}G - 2)G}{8} \cdot \frac{V_{\text{dc}}}{Lf_s} \quad \text{For MCPWM + 3P ST} \quad (74)$$

$$\Delta i_L = \frac{\sqrt{3}}{24} \frac{(\sqrt{3}G - 2)G}{\sqrt{3}G - 1} \cdot \frac{V_{\text{dc}}}{Lf_s} \quad \text{For MCPWM + 1P ST.} \quad (75)$$

B. Capacitor Requirement

As shown in Fig. 10, during ST interval, the discharging current of capacitor is i_L

$$i_{C\_\text{ST}}(\omega t) = -i_L. \quad (76)$$

The charging current of capacitor during non-ST interval is $i_L - i_{\text{dc}\_\text{link}}$, in which, $i_{\text{dc\_link}}$ changes among three-phase load current at different switching states. i_{C_NST} in the first sextant is expressed as

$$C\_\text{NST}(\omega t) = i_L - i_{\text{dc\_link}}(\omega t)$$

$$= \begin{cases} i_L & (111\,000) \\ i_L - \hat{i}_{ac}\cos(\omega t) & (100) \\ i_L + \hat{i}_{ac}\cos\left(\omega t + \frac{2\pi}{3}\right) & (110) \end{cases}. \quad (77)$$

The average current across the capacitor in one switching time period is zero. From (76), the capacitor voltage ripples for MCPWM + 1P/3P ST can be calculated based on d_{ST} and i_L

$$\Delta V_C = \frac{1}{C} \cdot i_L \cdot \frac{d_{\text{ST}}}{2}T_s \quad \text{For MCPWM + 3P ST} \quad (78)$$

$$\Delta V_C = \frac{1}{C} \cdot i_L \cdot \frac{d_{\text{ST}}}{6}T_s \quad \text{For MCPWM + 1P ST.} \quad (79)$$

Substituting i_L and d_{ST} in Table II into (78) and (79), the capacitor voltage ripples can be rewritten as

$$\Delta V_C = \frac{3}{16} \frac{(\sqrt{3}G - 2)G}{\sqrt{3}G - 1} \cdot \frac{\hat{i}_{ac}}{Cf_s} \quad \text{For MCPWM + 3P ST} \quad (80)$$

$$\Delta V_C = \frac{1}{16} \frac{(\sqrt{3}G - 2)G}{\sqrt{3}G - 1} \cdot \frac{\hat{i}_{ac}}{Cf_s} \quad \text{For MCPWM + 1P ST.} \quad (81)$$

Based on (76) and (77), the capacitor rms current ripples can be calculated as

$$I^2_{S\_\text{rms}} = \frac{6}{T_{\text{Line}}} \sum d(t) \cdot i^2_C(t)$$

$$= \frac{3}{\pi} \left[\int_0^{\pi/3} \begin{pmatrix} d_{\text{ST}}(\omega t) \cdot (-i_L)^2 + d_{(111\,000)}(\omega t) \cdot (i_L)^2 \\ + d_{(100)}(\omega t) \cdot (i_L - \hat{i}_{ac}(\omega t))^2 \\ + d_{(110)}(\omega t) \cdot \left(i_L + \hat{i}_{ac}\left(\omega t + \frac{2\pi}{3}\right)\right)^2 \end{pmatrix} d(\omega t) \right]. \quad (82)$$

(2) MPWM + 1P ST, MPWM + 3P ST, and IPWM + 1P ST
A. Inductor Requirement
The average voltage across the inductor in one switching time period can be derived as

$$\langle v_L(\omega t)\rangle_{T_s} = V_C \cdot d_{\text{ST}}(\omega t)T_s + (V_{\text{dc}} - V_C)(1 - d_{\text{ST}}(\omega t))T_s. \quad (83)$$

Substituting V_C and d_{st} in Table II into (83), $< v_L(\omega t) >_{T_s}$ can be simplified as

$$\langle v_L(\omega t)\rangle_{T_s} = \frac{\sqrt{3}G}{2}\left[\frac{3}{\pi} - \cos\left(\omega t - \frac{\pi}{6}\right)\right]. \quad (84)$$

As is shown in Fig. 18, the first sextant is divided into three time interval. During interval I $(\omega t_0, \omega t_1)$ and III $(\omega t_2, \omega t_3)$, when $< v_L >_{T_s} > 0$, i_L is increasing. During interval II

$(\omega t_1, \omega t_2)$, when $<v_L>_{T_s}<0$, i_L is decreasing. In one sextant, the average voltage across the inductor should be zero

$$\int_0^{\frac{\pi}{3}} \langle v_L(\omega t)\rangle_{T_s} d(\omega t) = 0. \tag{85}$$

The critical instants ωt_1 and ωt_2 for interval II can be calculated by assuming $\langle v_L(\omega t)\rangle_{T_s} = 0$

$$\begin{cases} \omega t_1 = -a\cos\left(\dfrac{3}{\pi}\right) + \dfrac{\pi}{6} \approx 0.2222 \\ \omega t_2 = a\cos\left(\dfrac{3}{\pi}\right) + \dfrac{\pi}{6} \approx 0.8250 \end{cases}. \tag{86}$$

Integrating $\langle v_L(\omega t)\rangle_{T_s}$ in (84) from ωt_1 to ωt_2, the inductor current ripples can be derived as

$$\Delta I_L \approx -\frac{1}{\omega L}\cdot\int_{0.2222}^{0.8250}\langle v_L(\omega t)\rangle_{T_s} d(\omega t) = \frac{0.0181}{\omega L}\cdot\frac{\sqrt{3}GV_{\mathrm{dc}}}{2}$$

$$= \frac{0.0184\sqrt{3}G}{4\pi}\cdot\frac{V_{\mathrm{dc}}}{Lf_{\mathrm{Line}}}. \tag{87}$$

B. Capacitor Requirement

Thus, the charging current of capacitor during non-ST interval i_{C_NST} is as

$$i_{C\_\mathrm{NST}}(\omega t) = i_L - i_{\mathrm{dc\_link}}(\omega t)$$

$$= \begin{cases} i_L - \hat{i}_{\mathrm{ac}}\cos(\omega t) & (100) \\ i_L + \hat{i}_{\mathrm{ac}}\cos\left(\omega t + \dfrac{2\pi}{3}\right) & (110) \end{cases}. \tag{88}$$

From (76) and (88), the average current across the capacitor in one switching time period can be derived and simplified as

$$\langle i_C(\omega t)\rangle_{Ts} = d_{\mathrm{ST}}(\omega t)\cdot(-i_L) + d_{(100)}(\omega t)\cdot(i_L - \hat{i}_{\mathrm{ac}}(\omega t))$$

$$+ d_{(110)}(\omega t)\cdot\left(i_L + \hat{i}_{\mathrm{ac}}\left(\omega t + \frac{2\pi}{3}\right)\right)$$

$$= \frac{3\sqrt{3}\pi G^2\hat{i}_{\mathrm{ac}}}{4(3\sqrt{3}G-\pi)}\left[\cos\left(\omega t - \frac{\pi}{6}\right) - \frac{3}{\pi}\right]. \tag{89}$$

v_C increases during interval II, the critical instants ωt_1 and ωt_2 can be calculated by assuming $\langle i_C(\omega t)\rangle_{T_s} = 0$. Obviously, the critical instants ωt_1 and ωt_2 are the same as (86). Similarly, integrating $\langle i_C(\omega t)\rangle_{T_s}$ in (89) from ωt_1 to ωt_2, the capacitor voltage ripples can be derived as

$$\Delta v_C \approx \frac{1}{\omega C}\cdot\int_{0.2222}^{0.8250}\langle i_C(\omega t)\rangle_{T_s} d(\omega t)$$

$$= \frac{0.0181}{2\pi f_{\mathrm{Line}}C}\cdot\frac{3\sqrt{3}\pi G^2\hat{i}_{\mathrm{ac}}}{4(3\sqrt{3}G-\pi)}$$

$$= \frac{0.0181\cdot 3\sqrt{3}\pi G^2}{8\pi(3\sqrt{3}G-\pi)}\frac{\hat{i}_{\mathrm{ac}}}{f_{\mathrm{line}}C}. \tag{90}$$

The capacitor rms current ripples can be calculated as

$$I_{S\_\mathrm{rms}}^2 = \frac{6}{T_{\mathrm{Line}}}\sum d(t)\cdot i_C^2(t)$$

$$= \frac{3}{\pi}\left[\int_0^{\pi/3}\begin{pmatrix} d_{\mathrm{ST}}(\omega t)\cdot(-i_L)^2 + d_{(100)}(\omega t) \\ \cdot(i_L - \hat{i}_{\mathrm{ac}}(\omega t))^2 \\ + d_{(110)}(\omega t)\cdot\left(i_L + \hat{i}_{\mathrm{ac}}\left(\omega t + \dfrac{2\pi}{3}\right)\right)^2 \end{pmatrix} d(\omega t)\right]. \tag{91}$$

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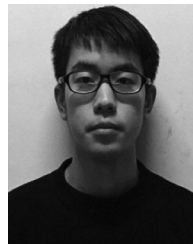
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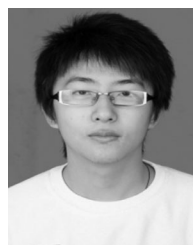
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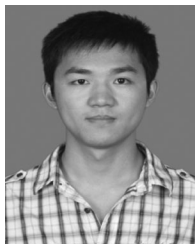
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